

FIG. 1

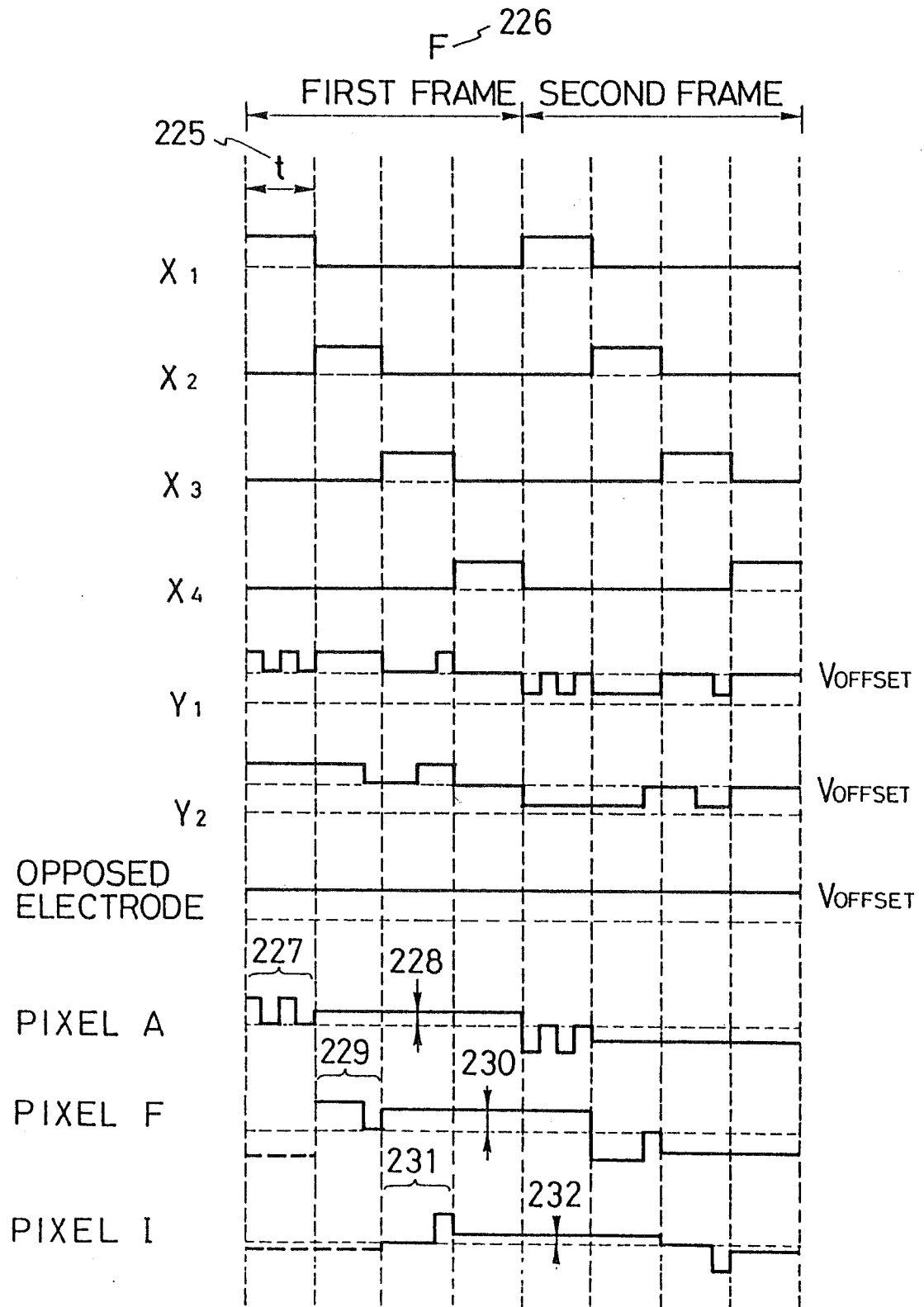


FIG. 2

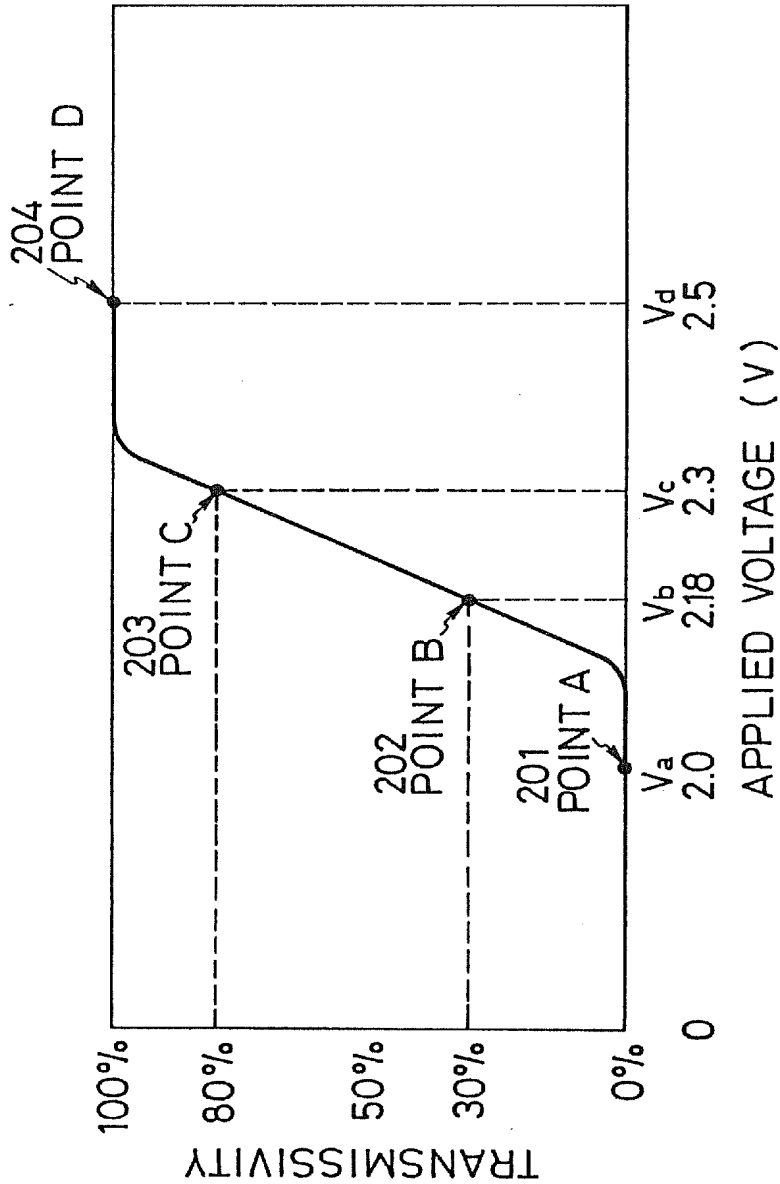
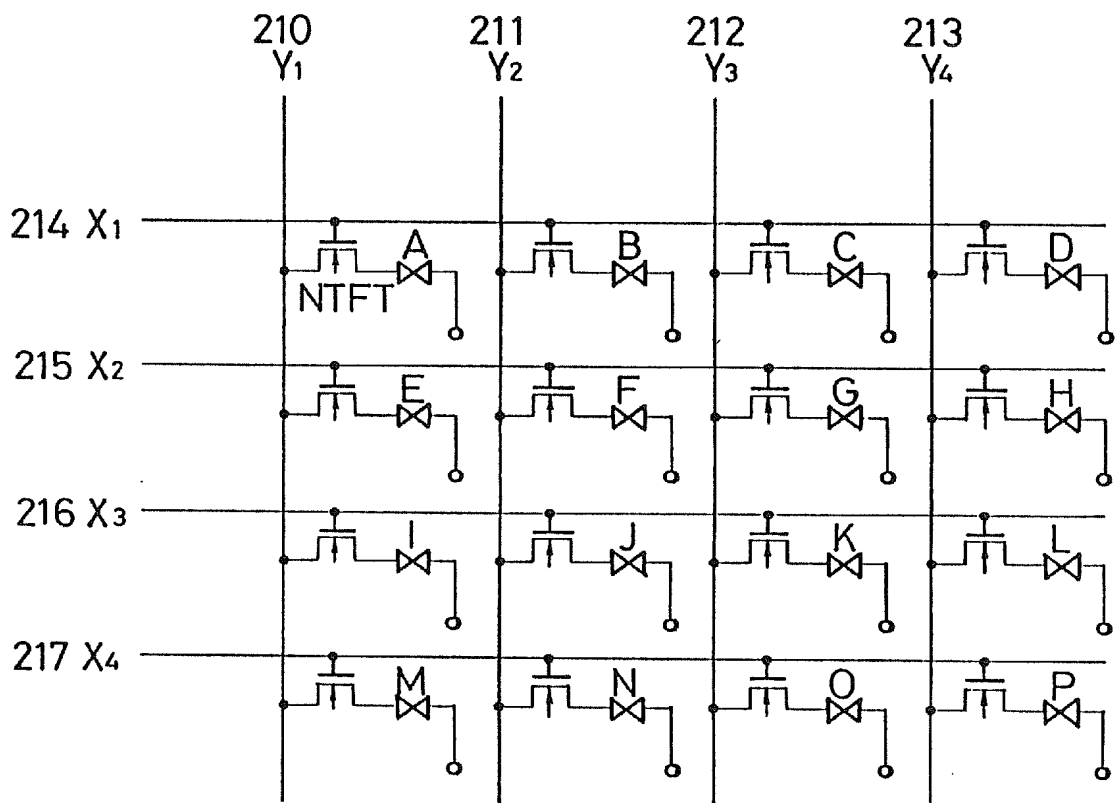


FIG. 3



PRIOR ART
FIG. 4

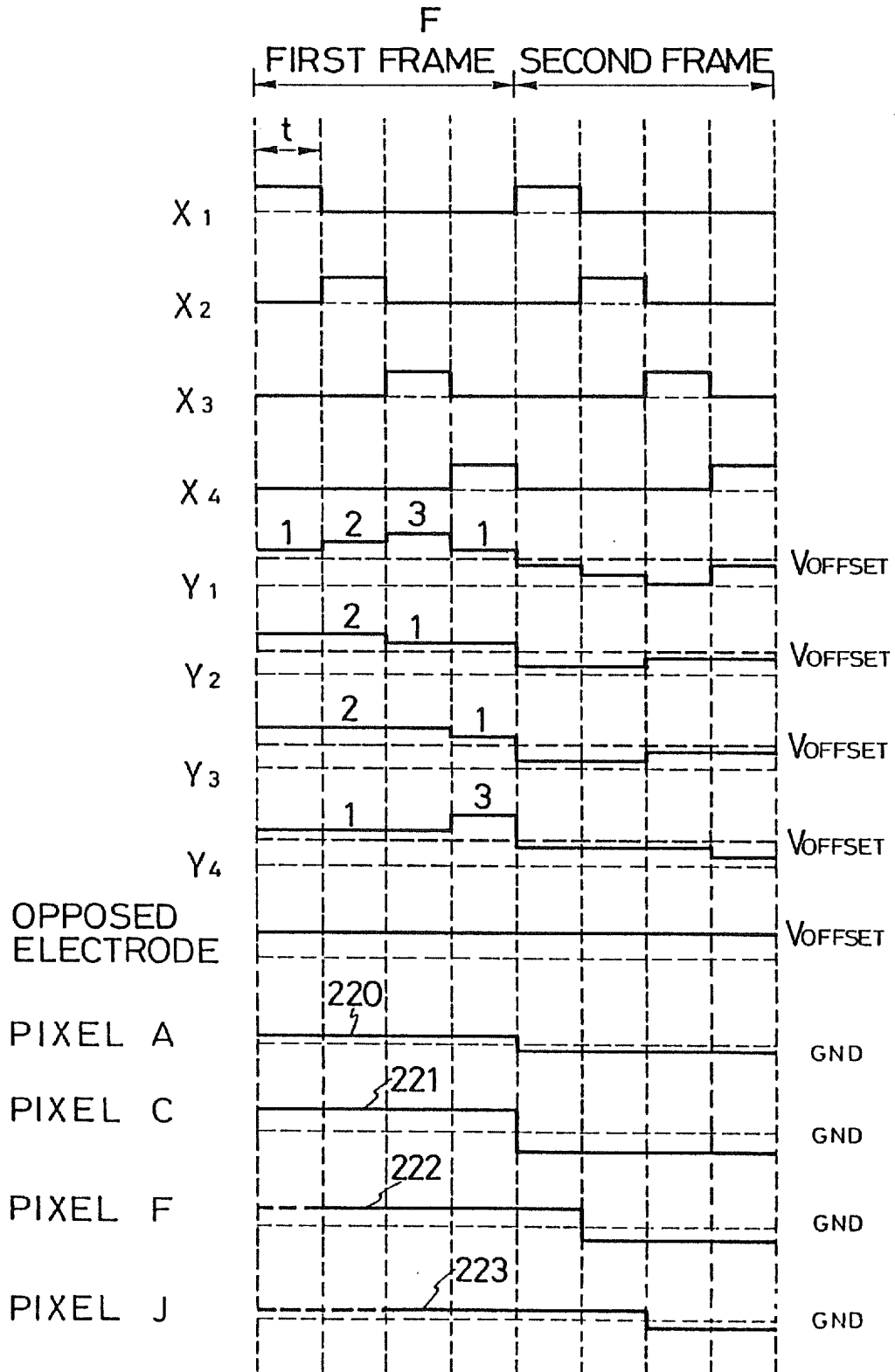


FIG. 5

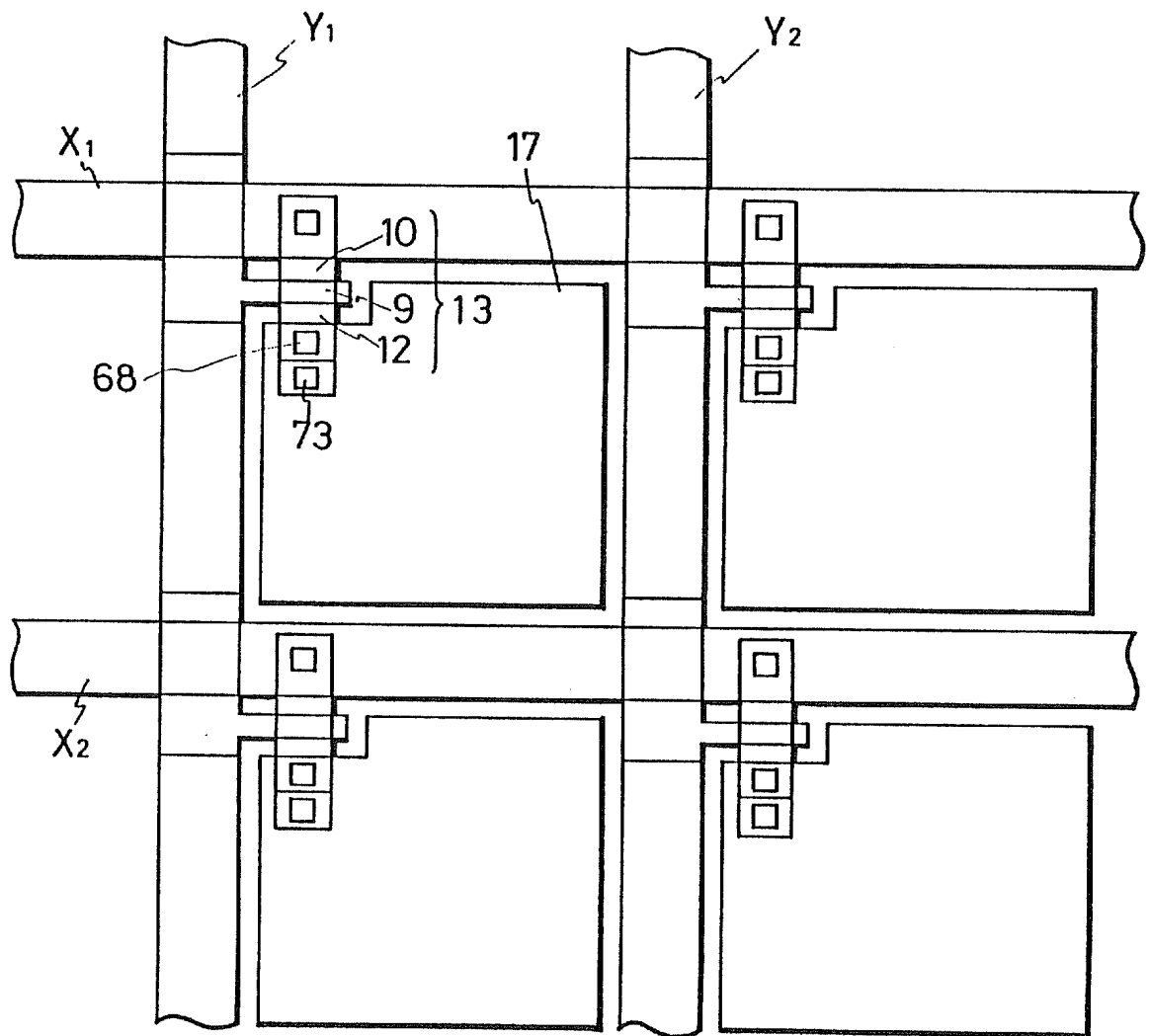


FIG. 6(A)

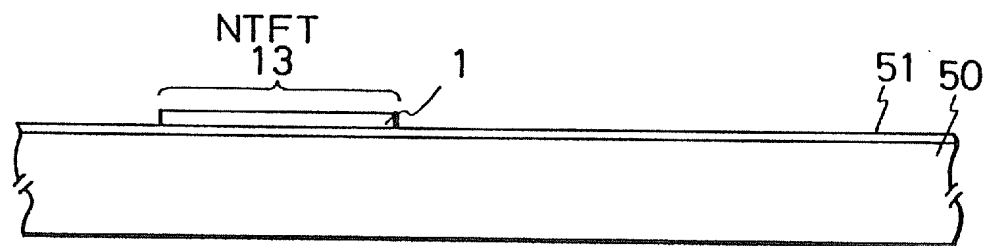


FIG. 6(B)

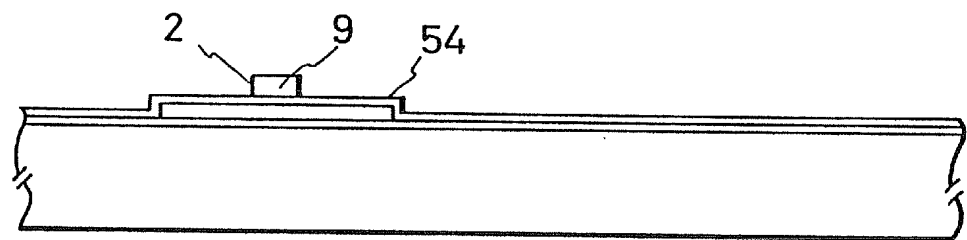


FIG. 6(C)

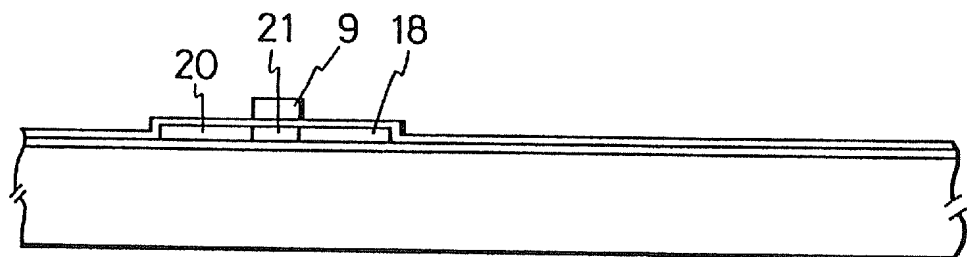


FIG. 6(D)

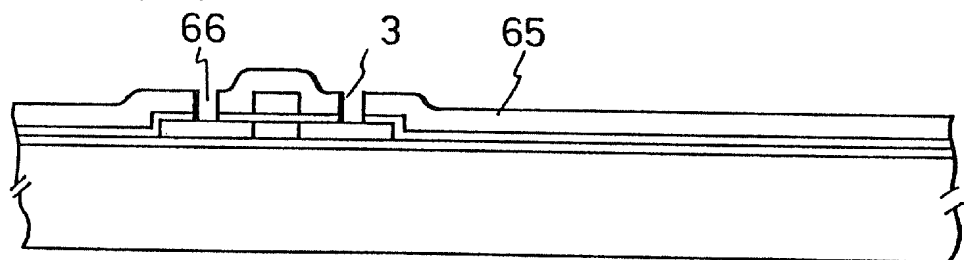


FIG. 6(E)

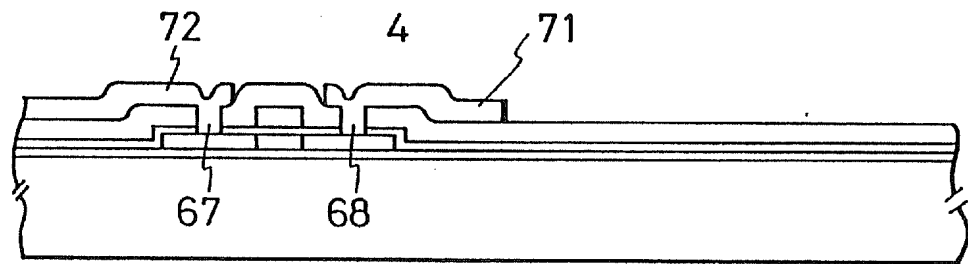


FIG. 6(F)

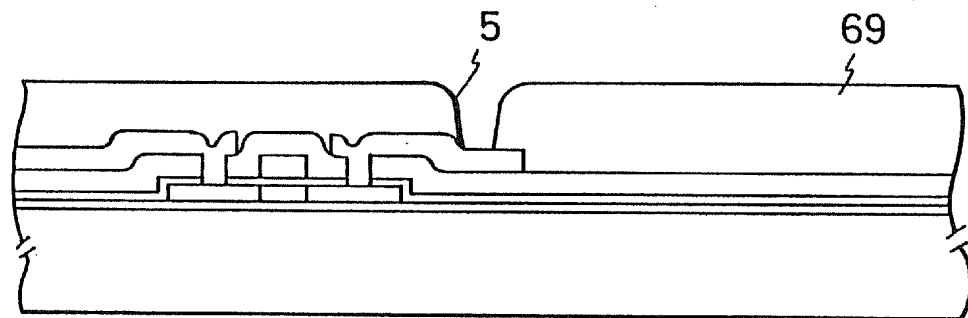


FIG. 6(G)

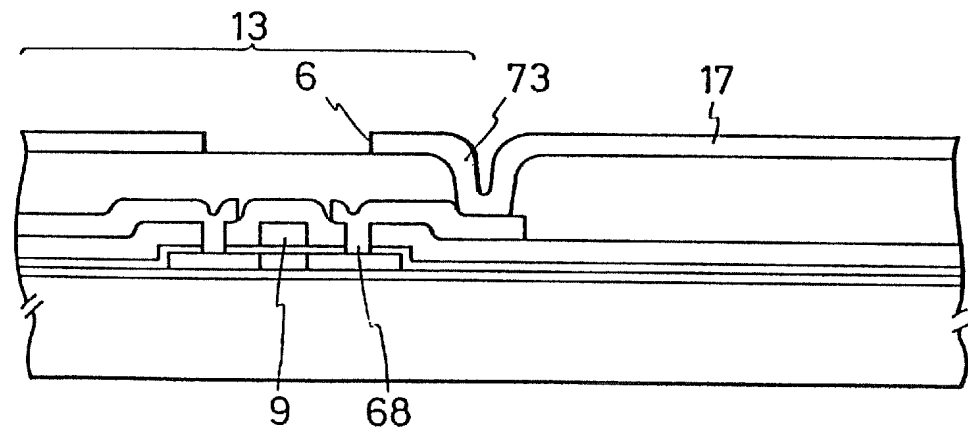
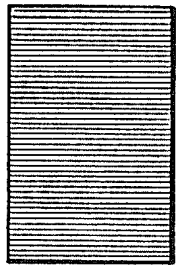
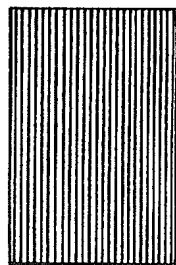


FIG. 7

PIXEL A



PIXEL F



PIXEL I

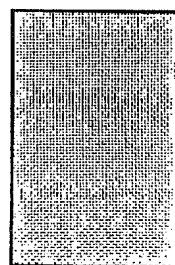


FIG. 8

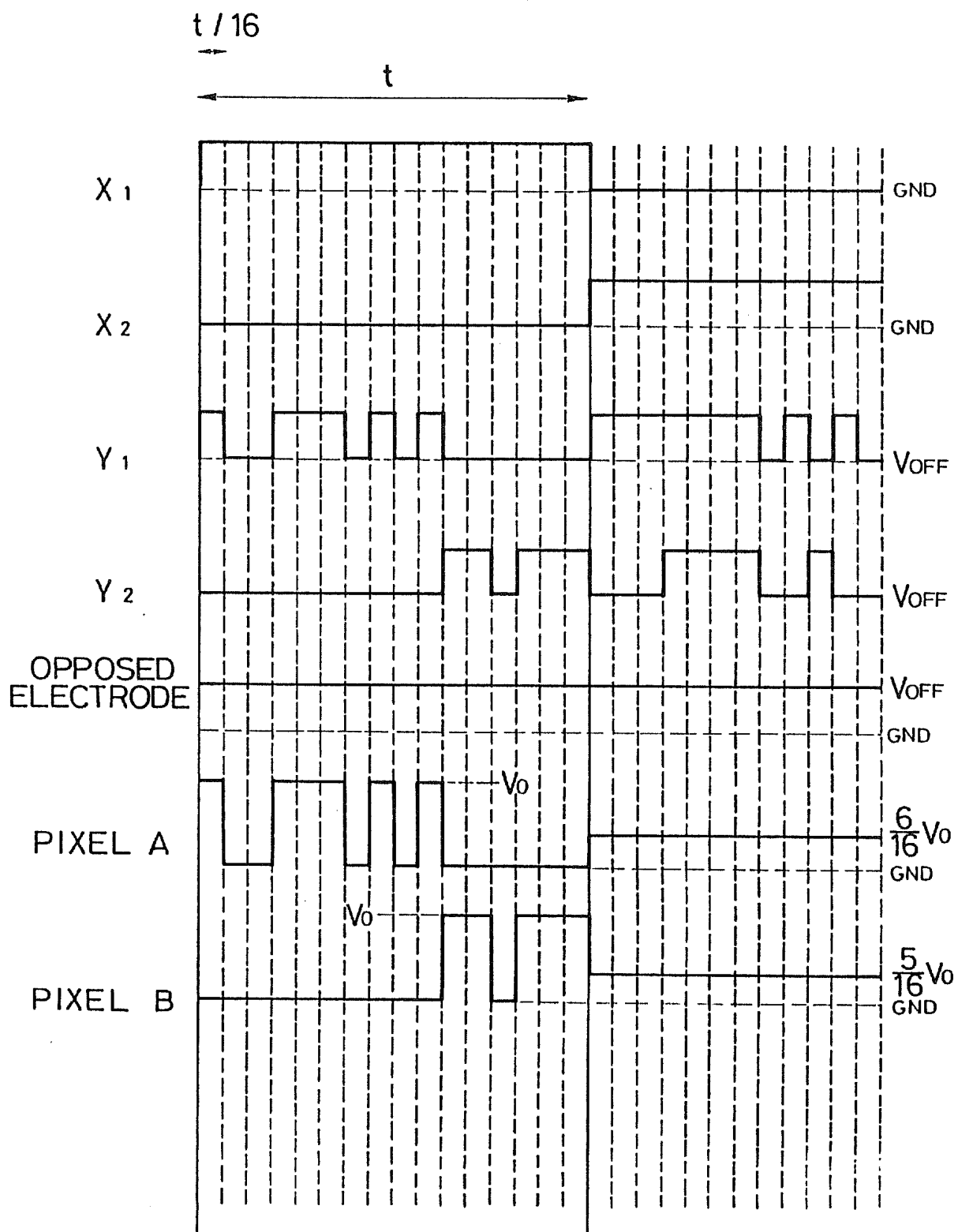


FIG. 9

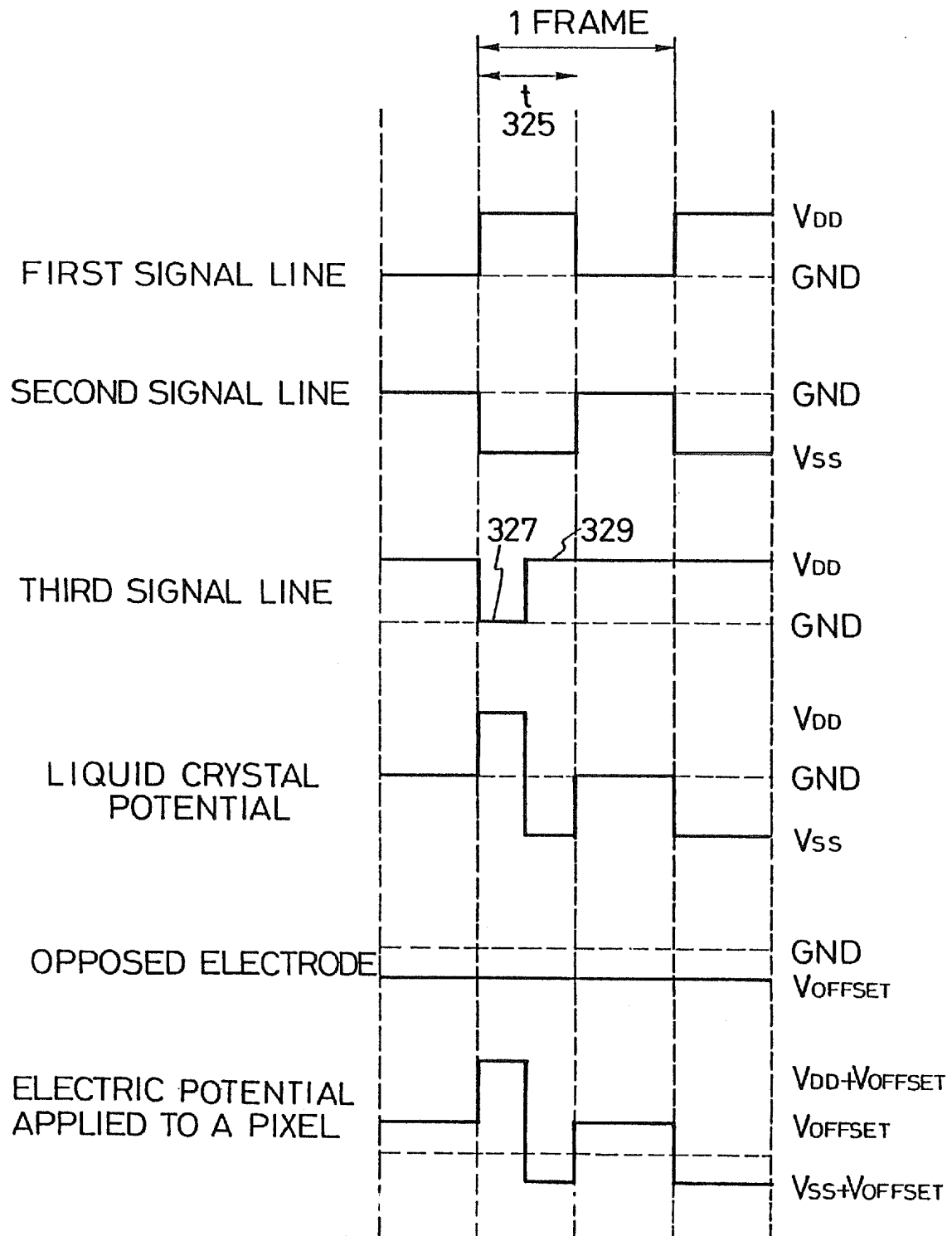
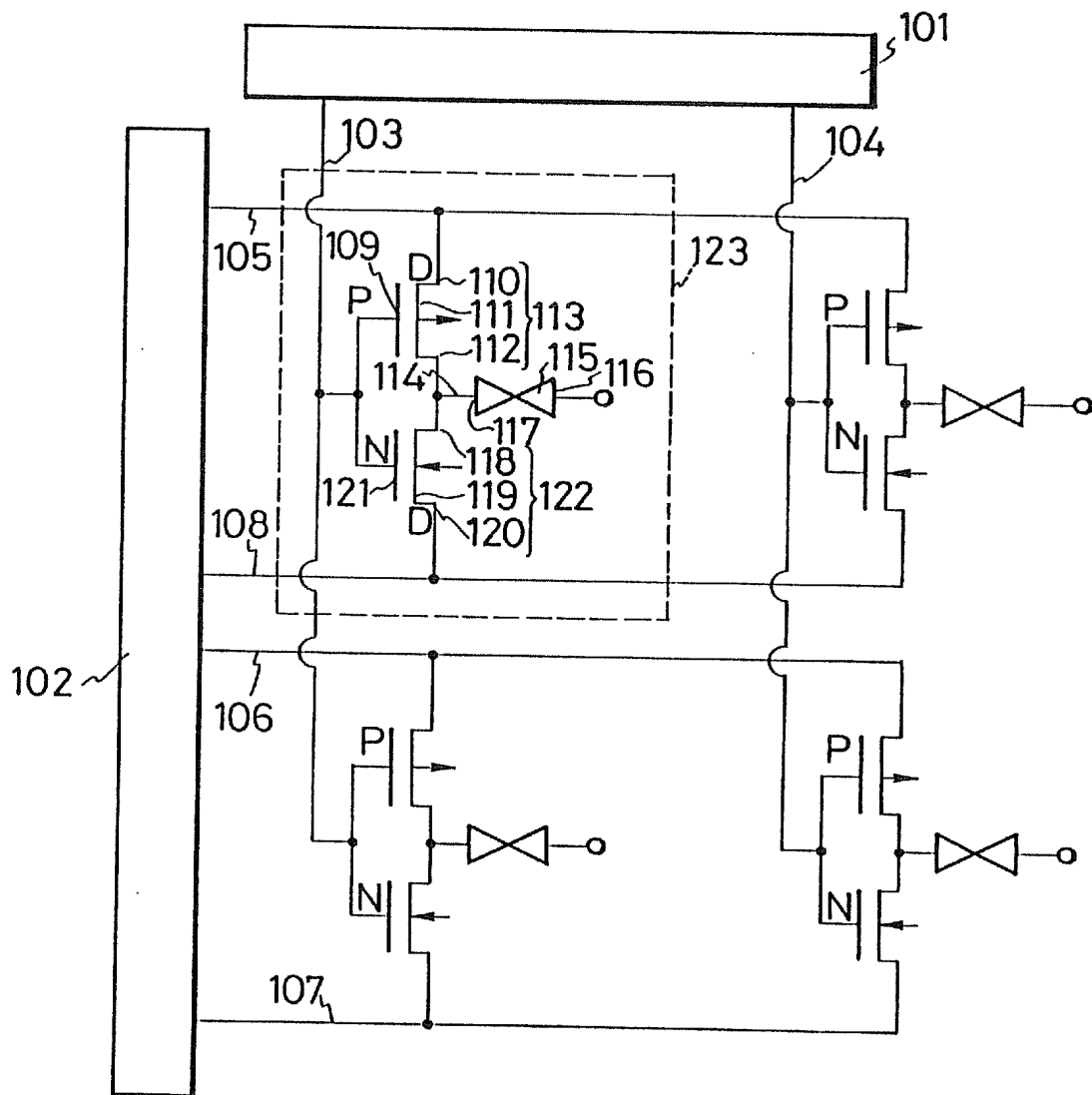


FIG. 10



PRIOR ART
FIG. 11

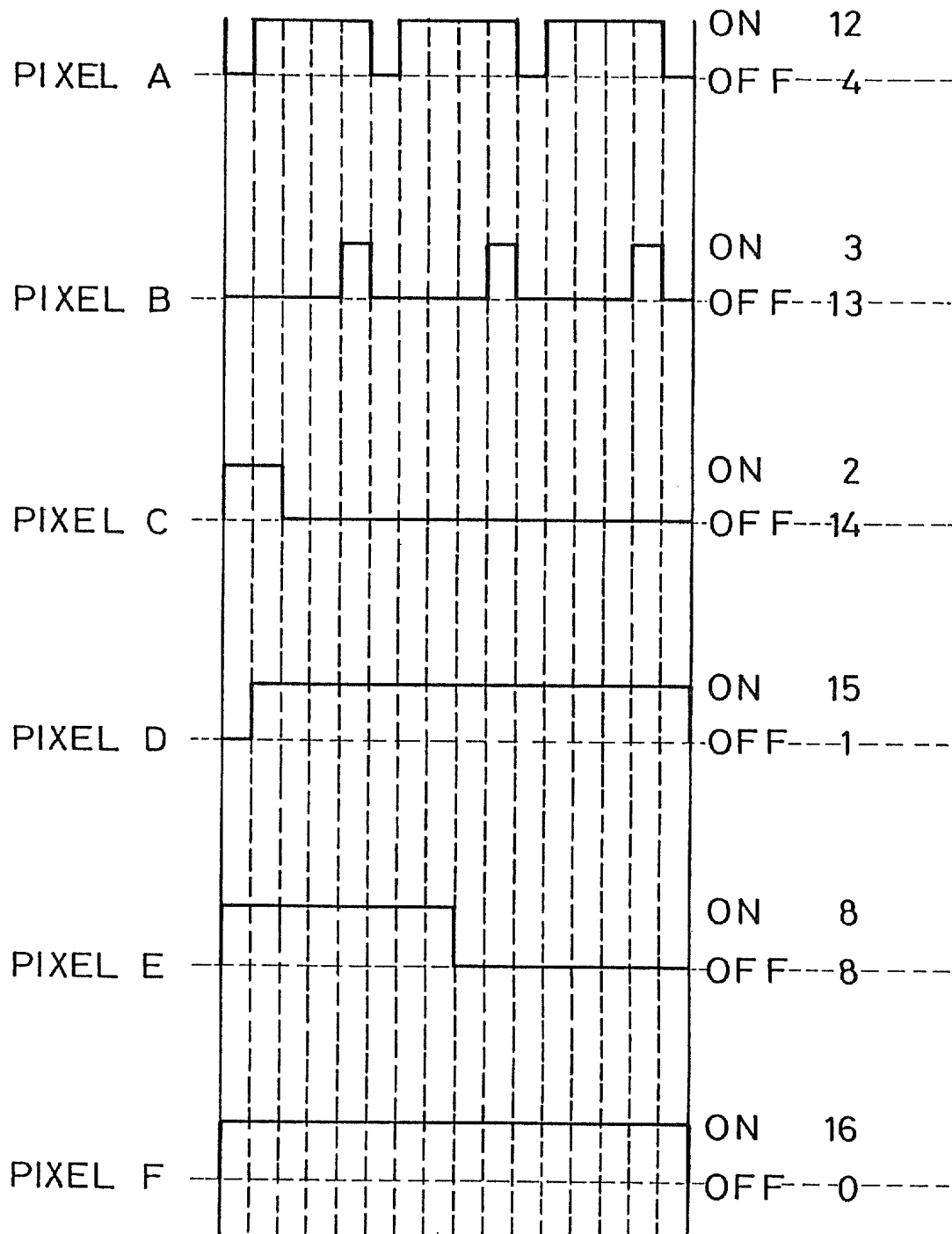


FIG. 12

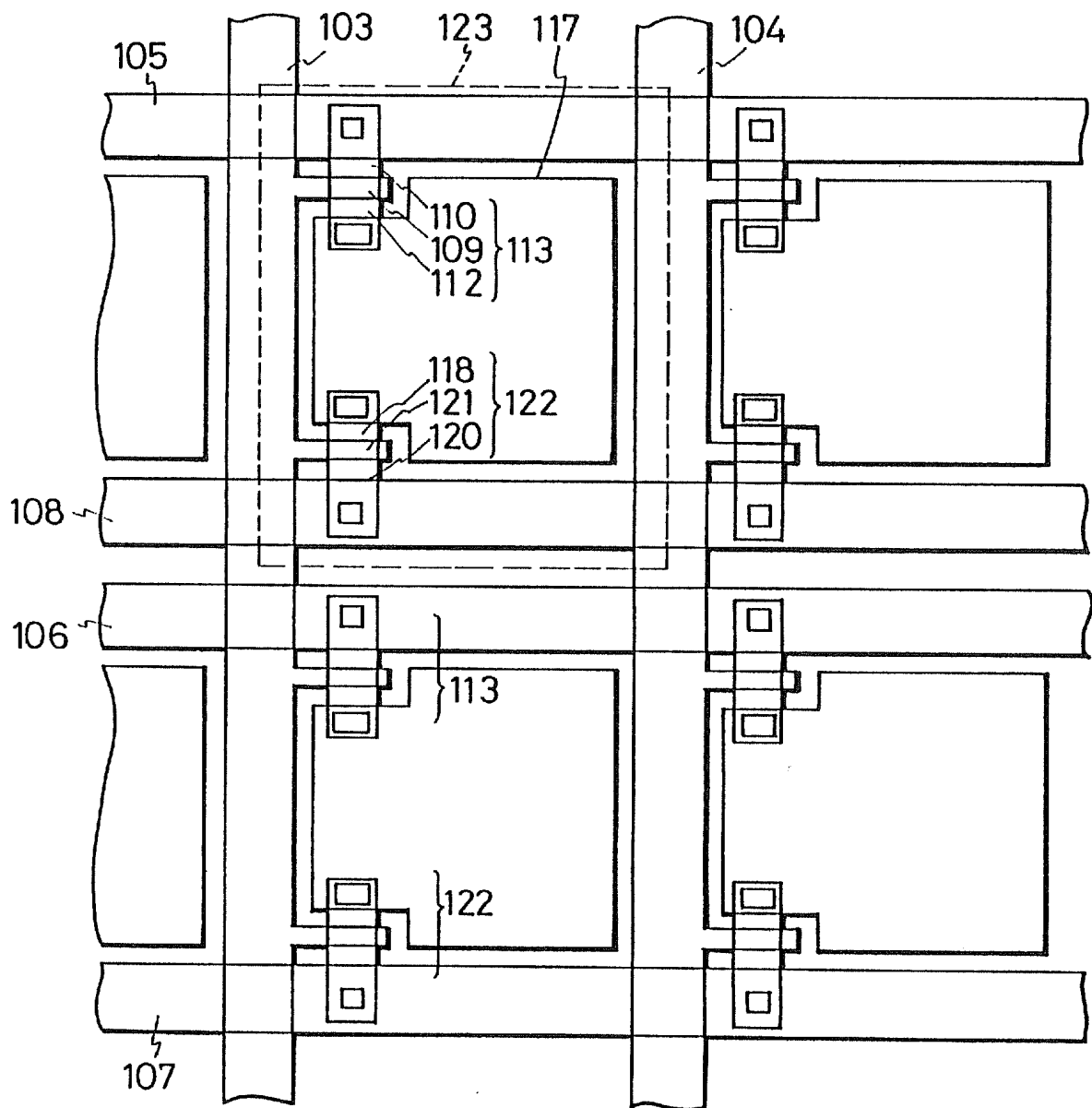


FIG. 13(A)

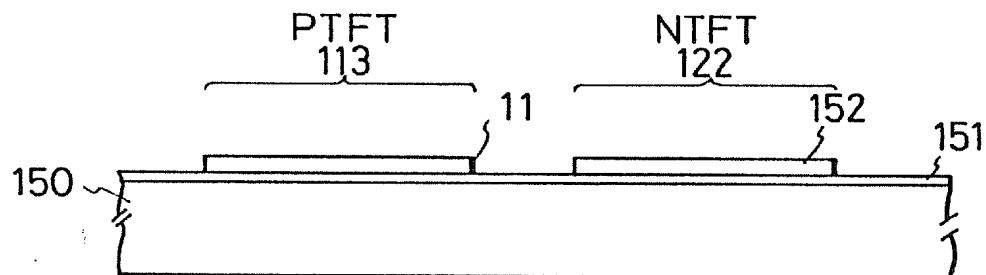


FIG. 13(B)

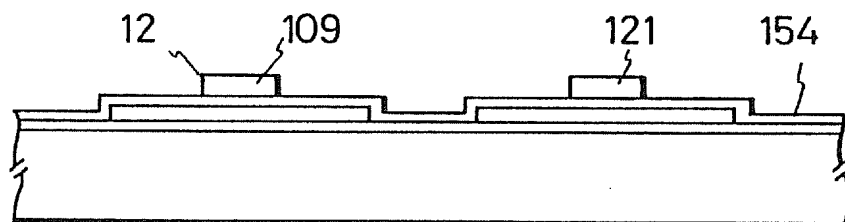


FIG. 13(C)

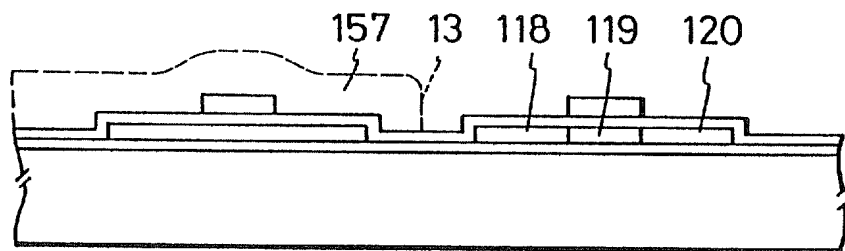


FIG. 13(D)

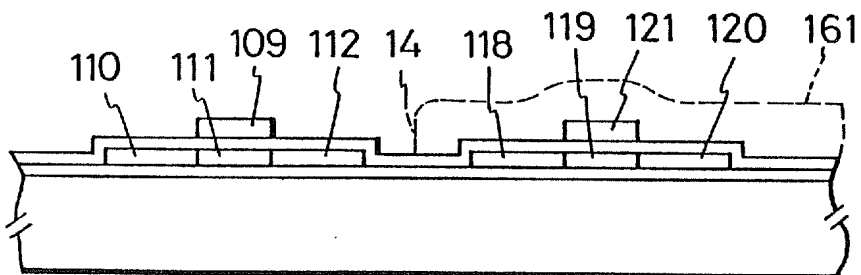


FIG. 13(E)

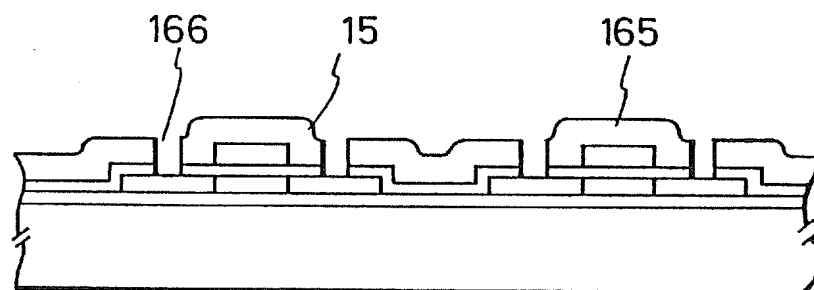


FIG. 13(F)

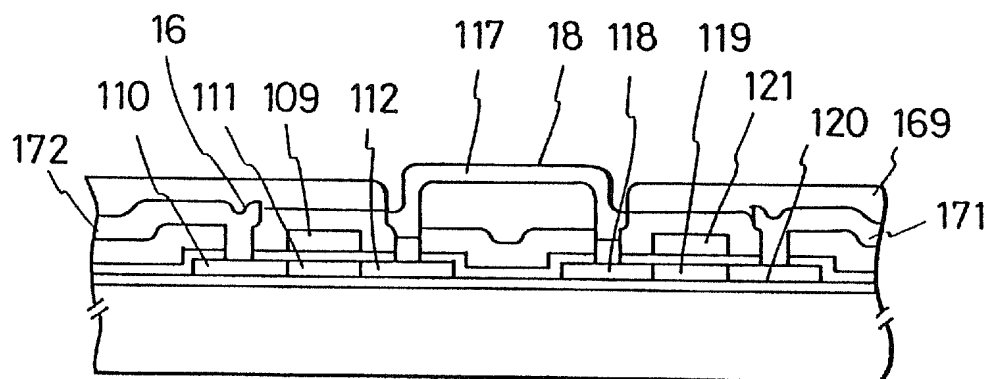
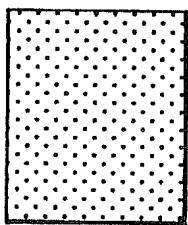
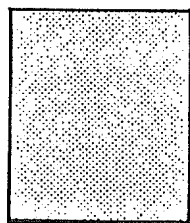


FIG. 14

PIXEL A



PIXEL E



PIXEL C

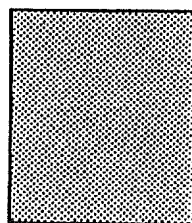


FIG. 15

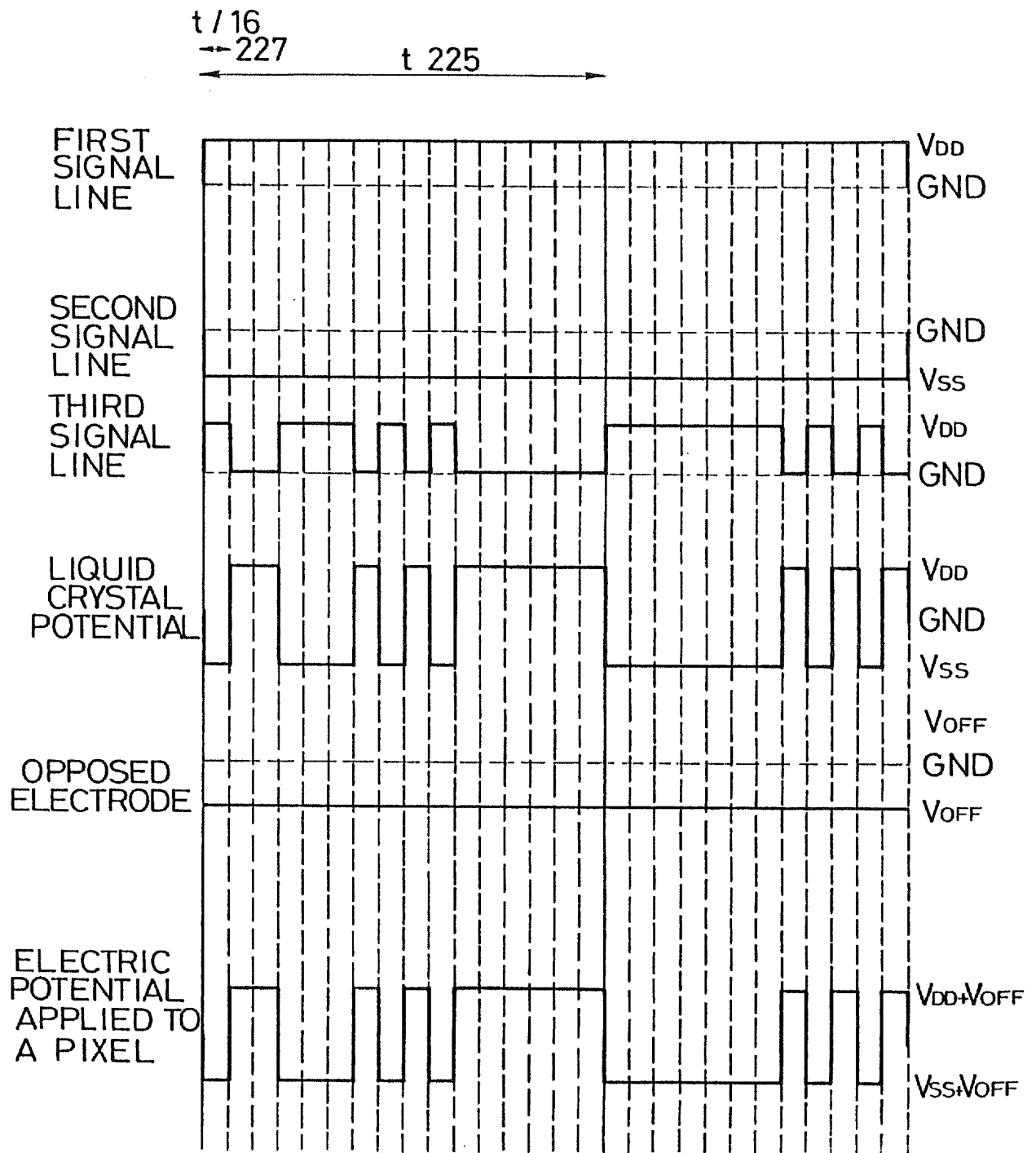


FIG. 16

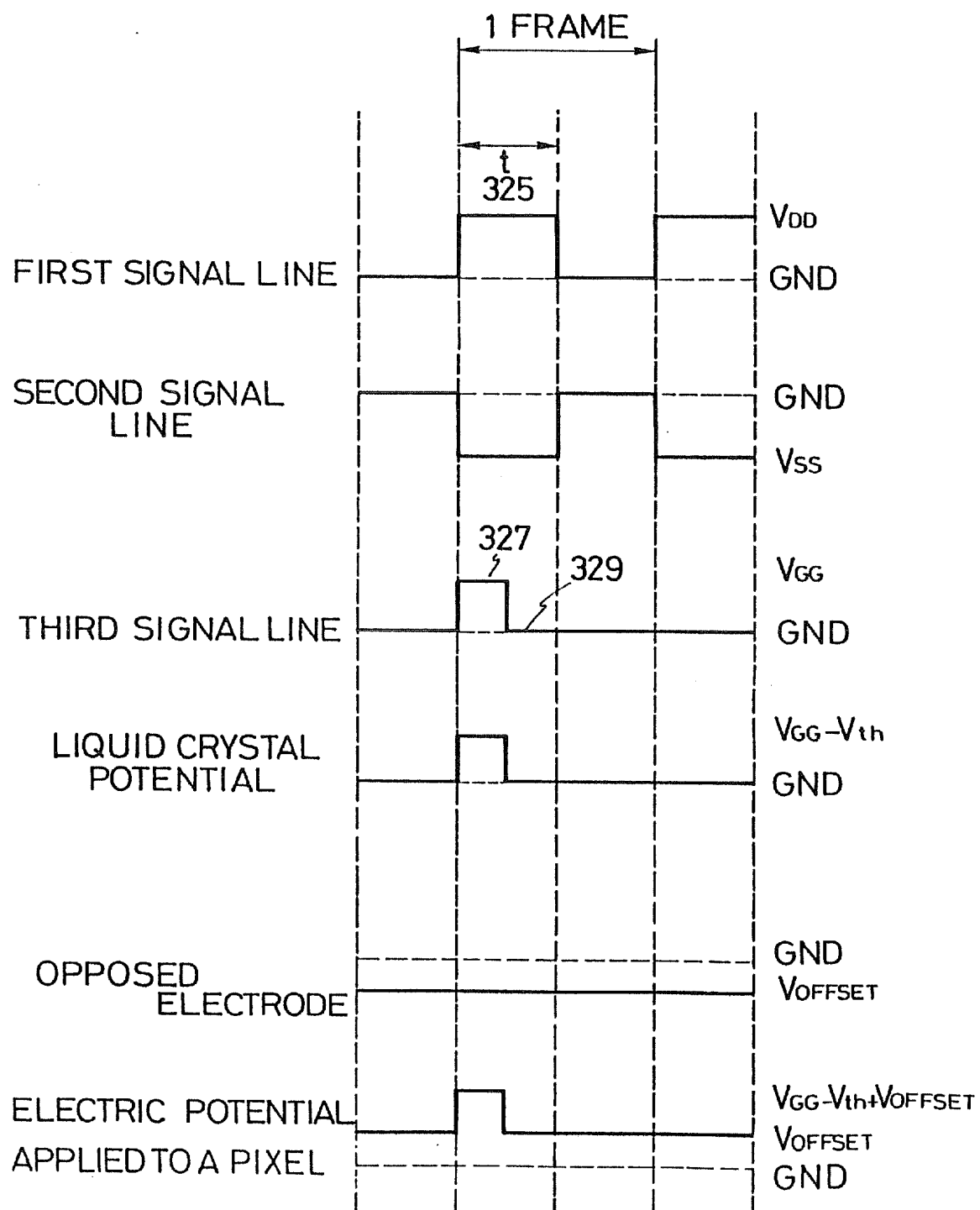


FIG. 17

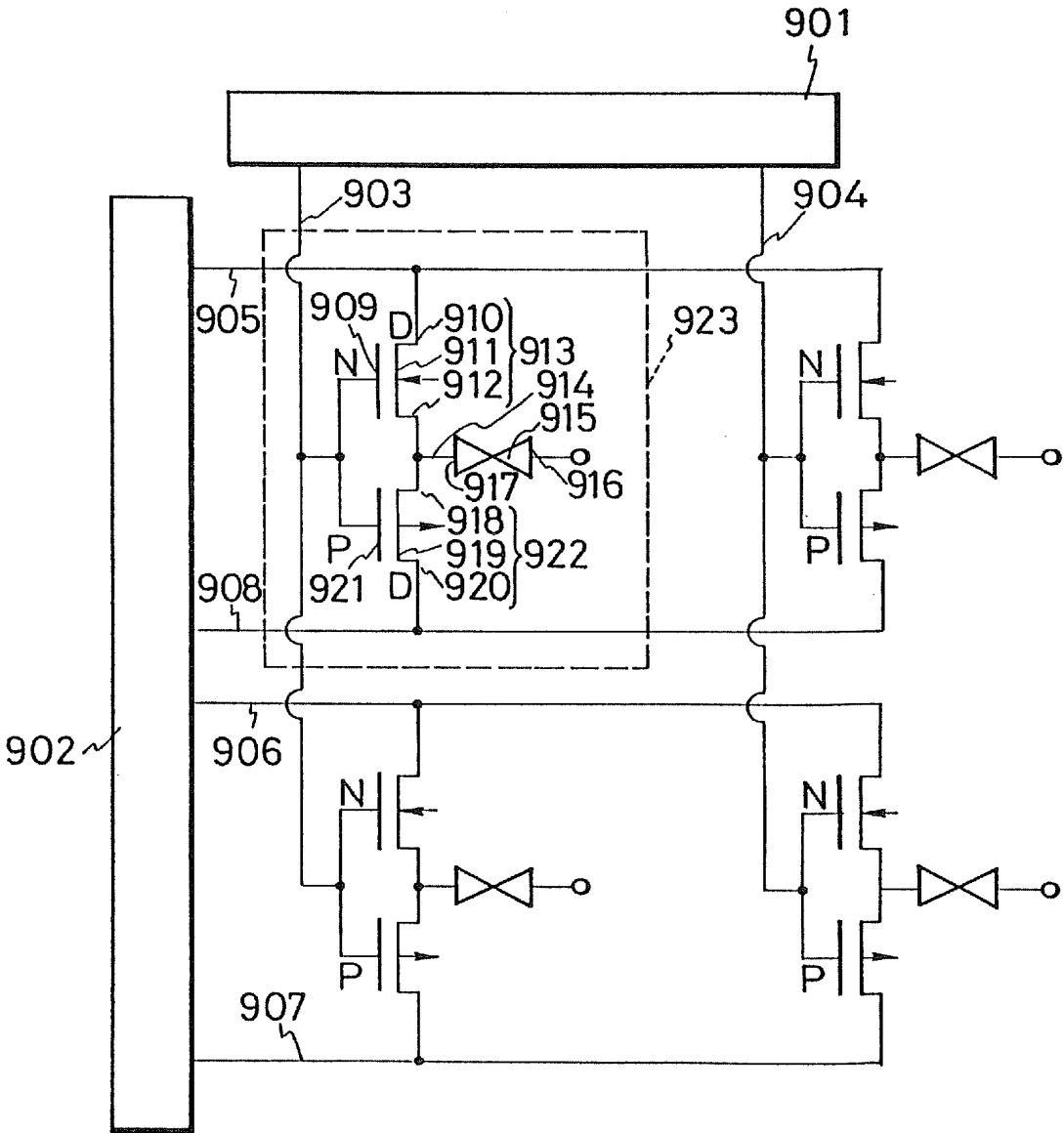


FIG. 18(A)

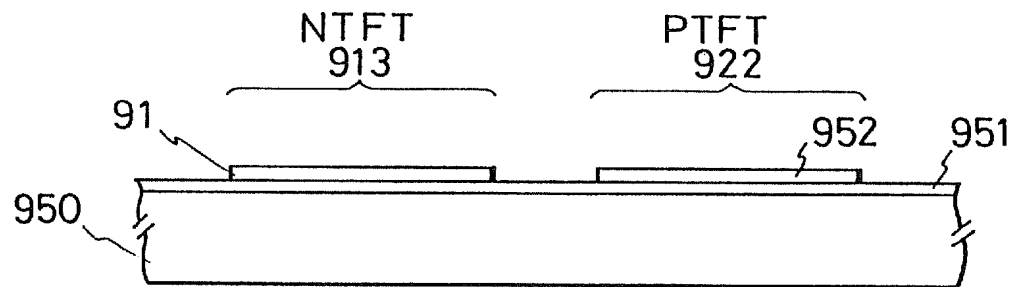


FIG. 18(B)

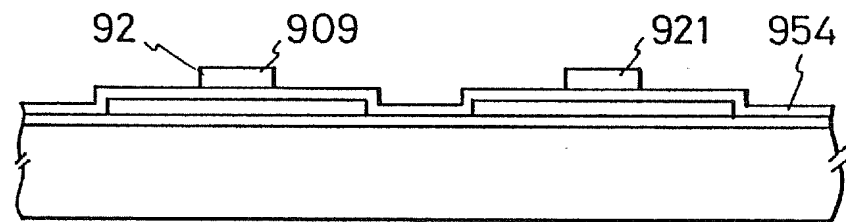


FIG. 18(C)

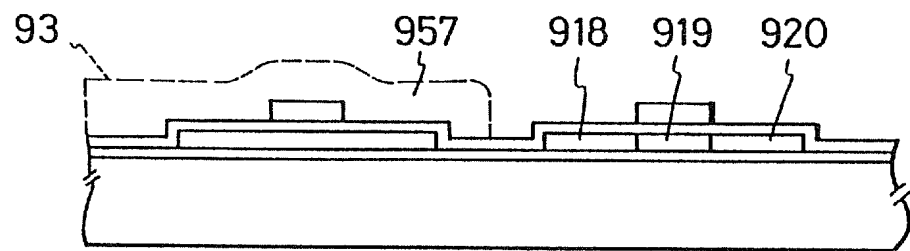


FIG. 18(D)

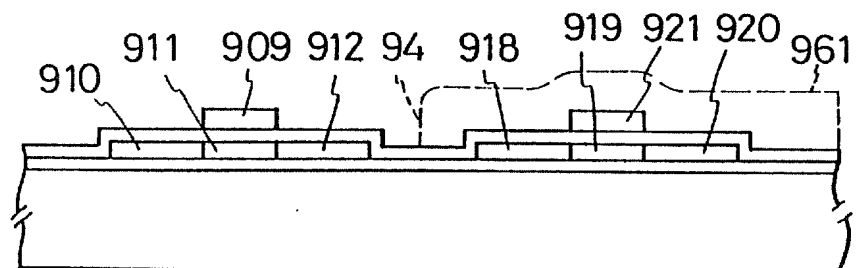


FIG. 18(E)

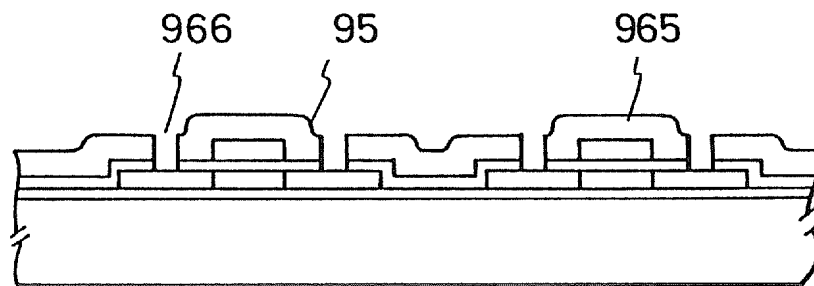


FIG. 18(F)

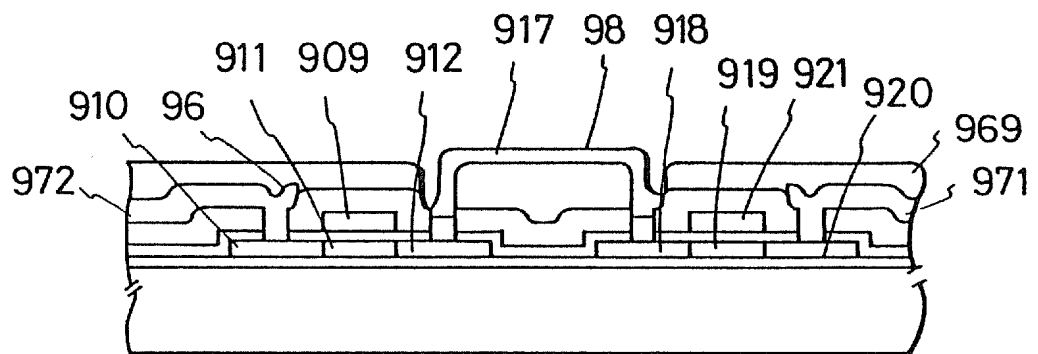


FIG. 19

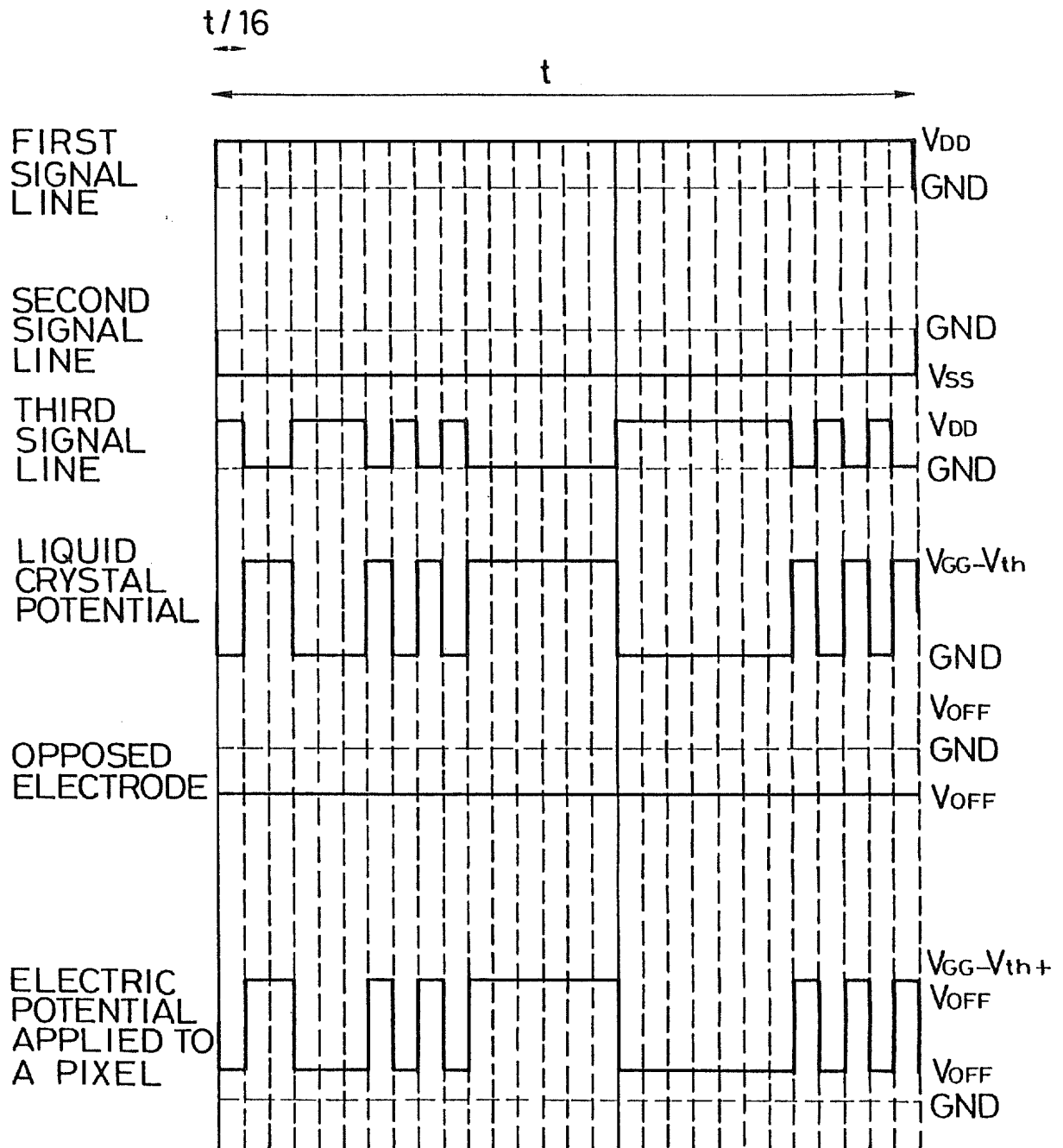


FIG. 20

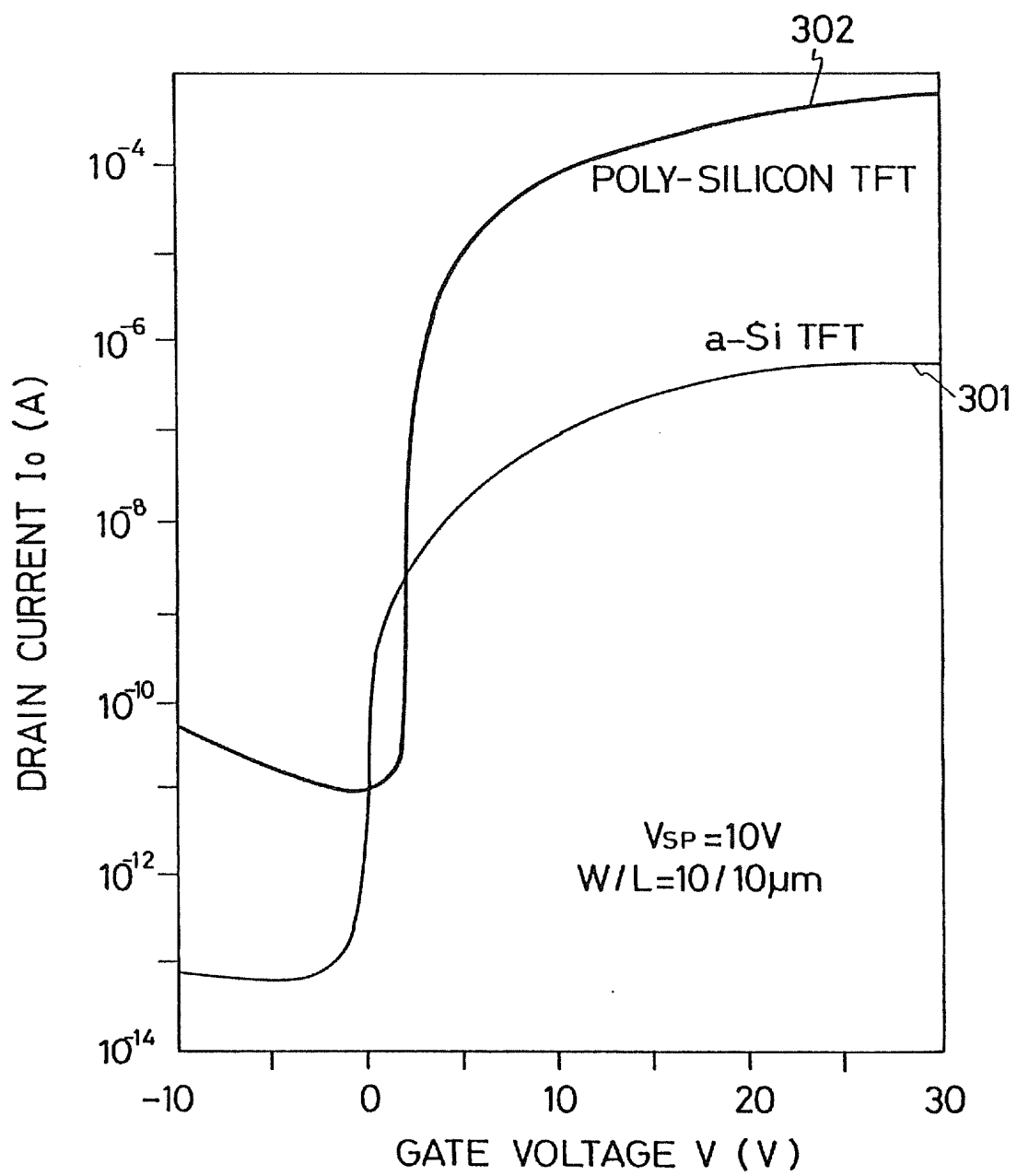


FIG. 21

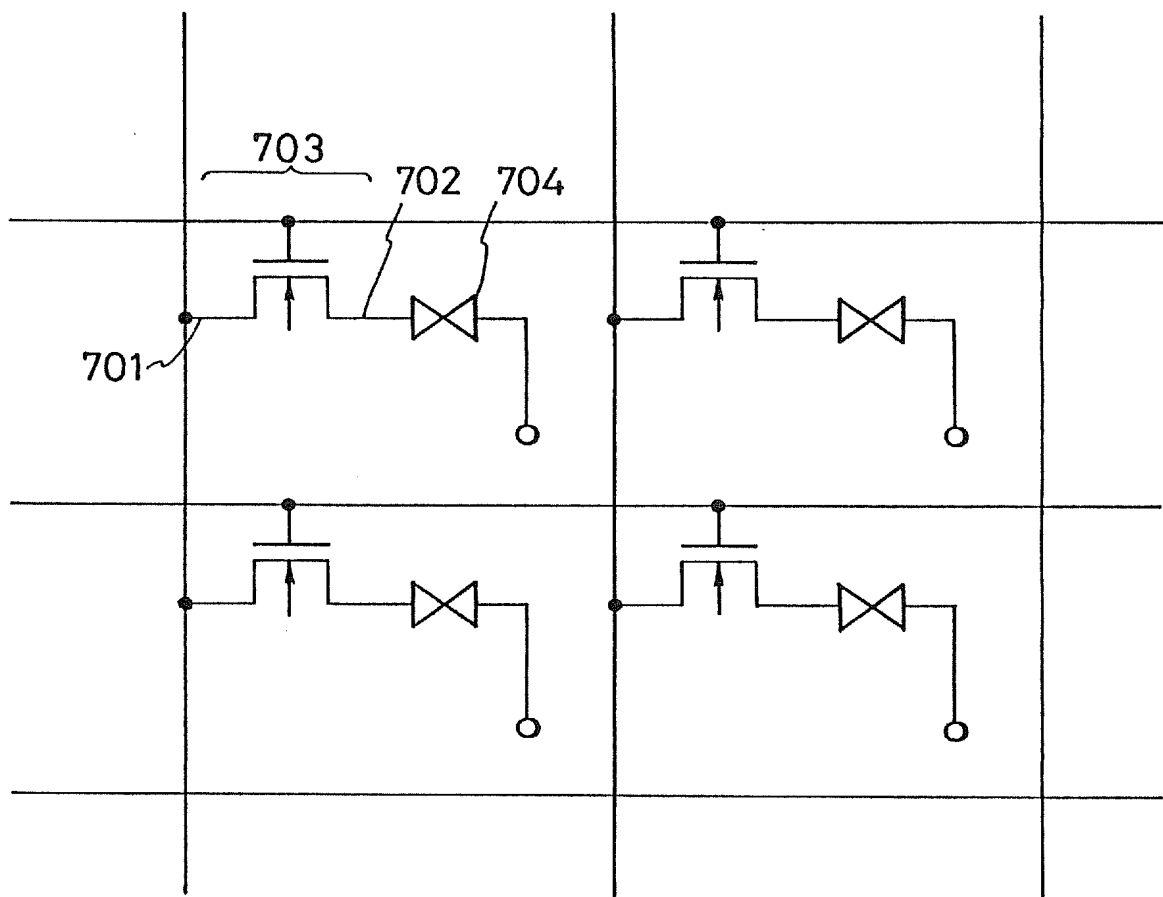


FIG. 22(A)

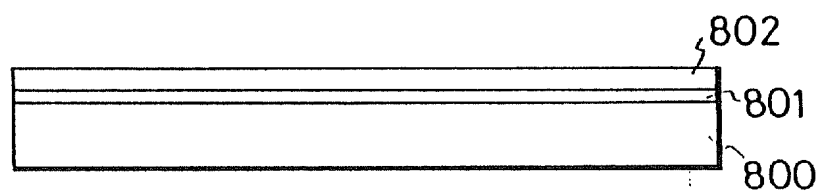


FIG. 22(B)

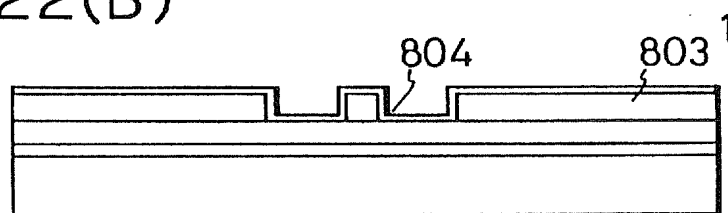


FIG. 22(C)

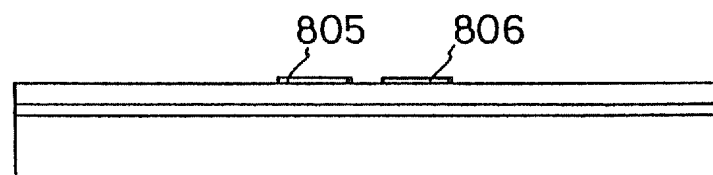


FIG. 22(D)

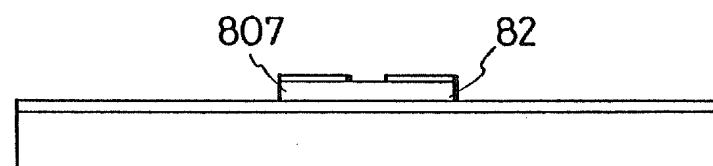


FIG. 22(E)

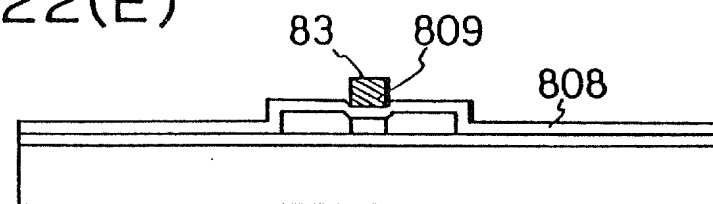


FIG. 22(F)

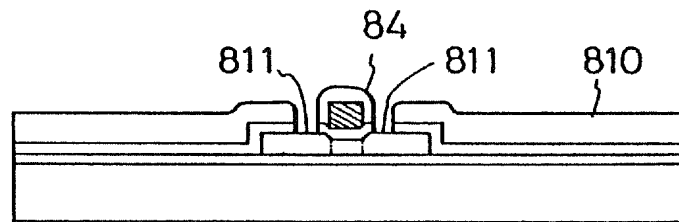


FIG. 22(G)

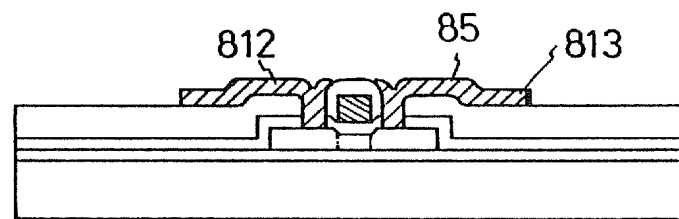


FIG. 22(H)

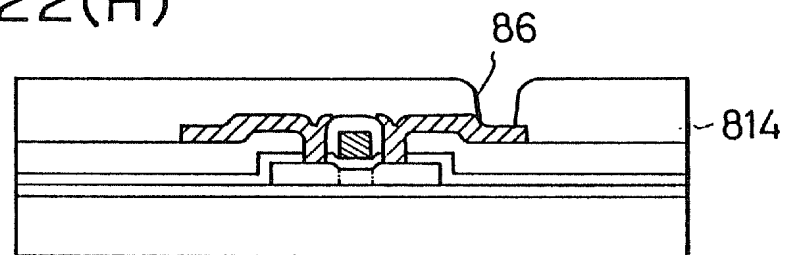


FIG. 22(I)

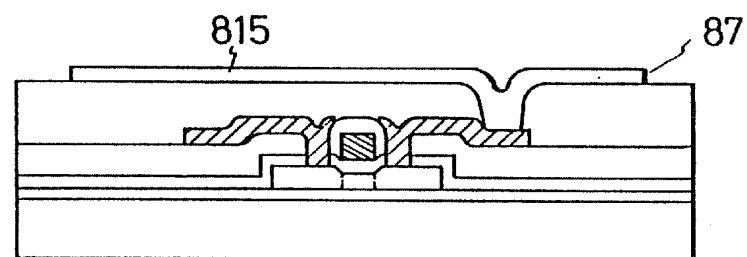


FIG. 23(A)

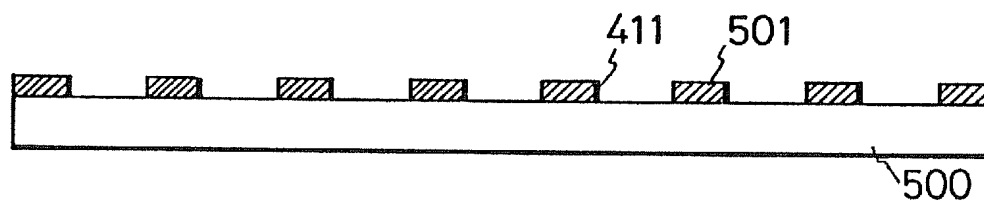


FIG. 23(B)

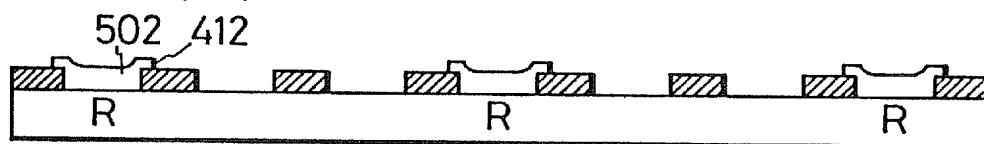


FIG. 23(C)

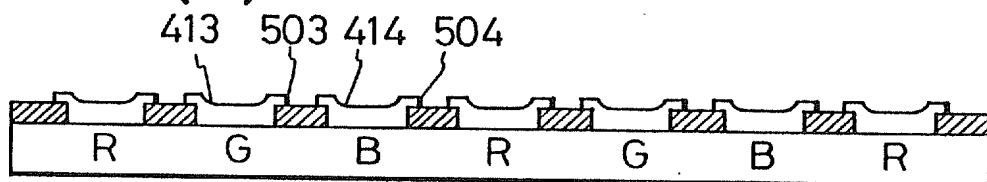


FIG. 23(D)

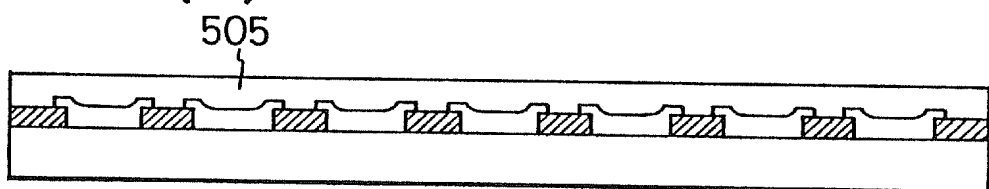


FIG. 23(E)

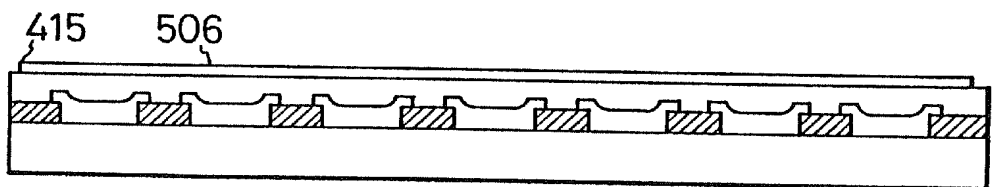


FIG. 24

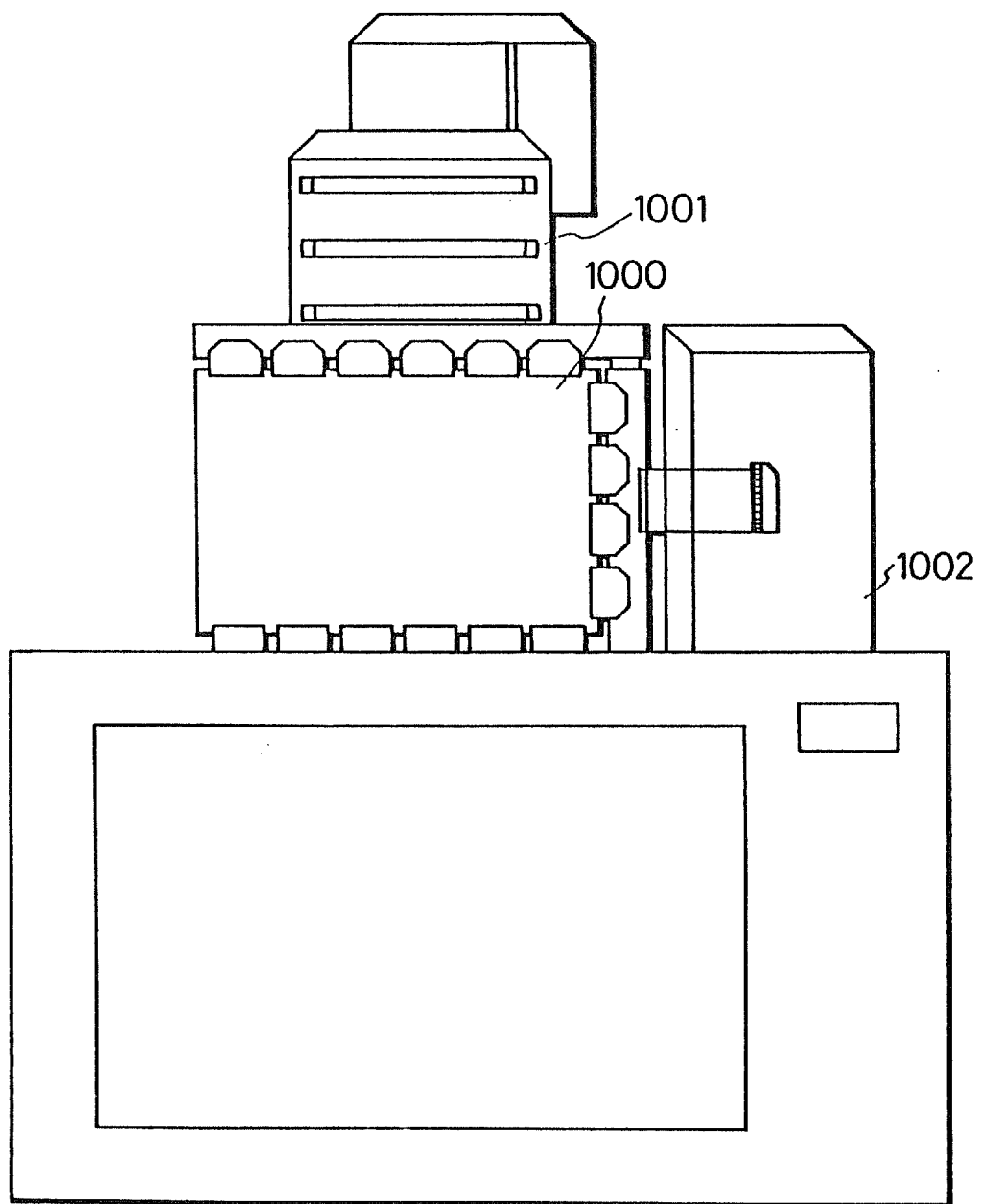


FIG. 25

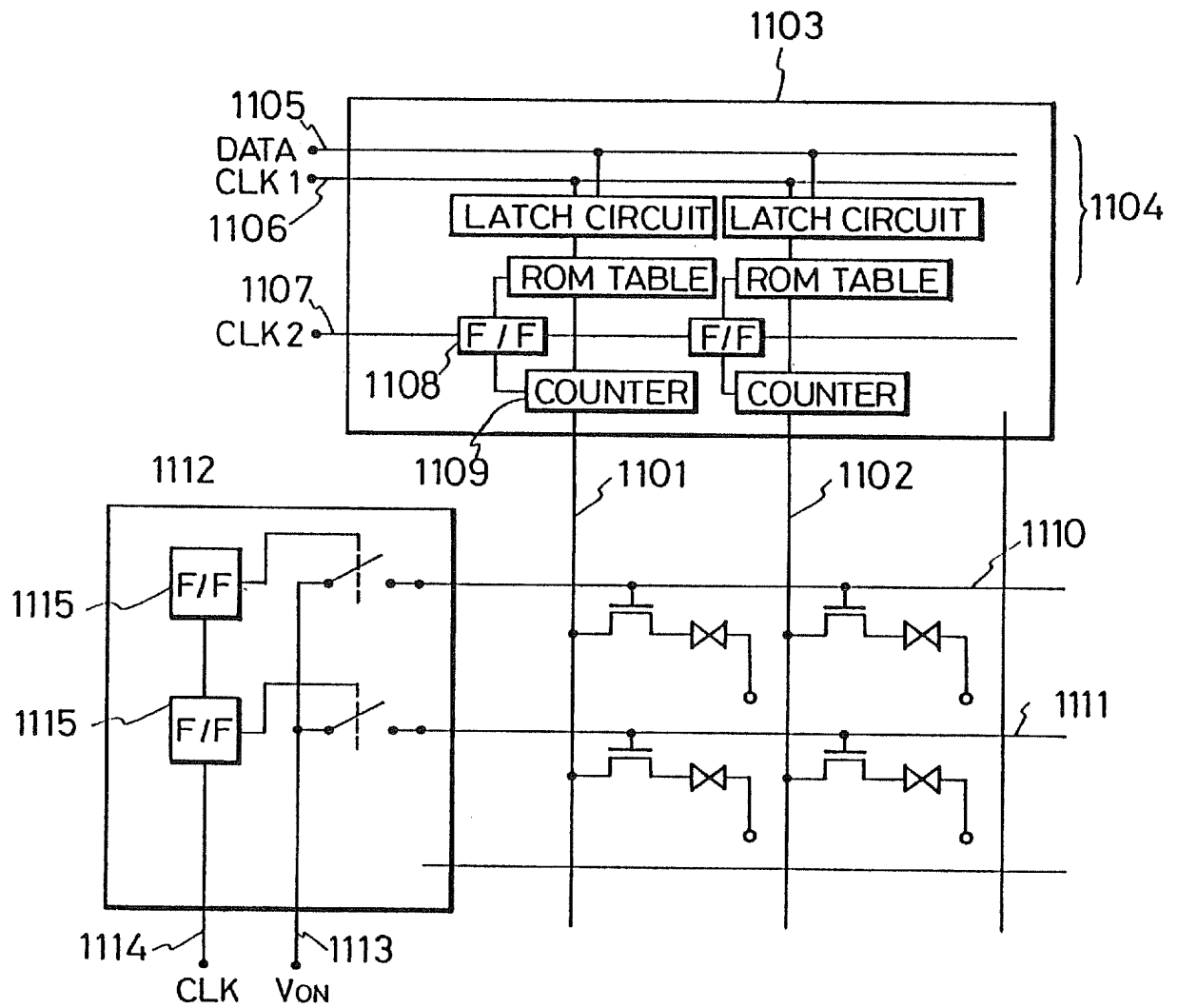


FIG. 26(A)

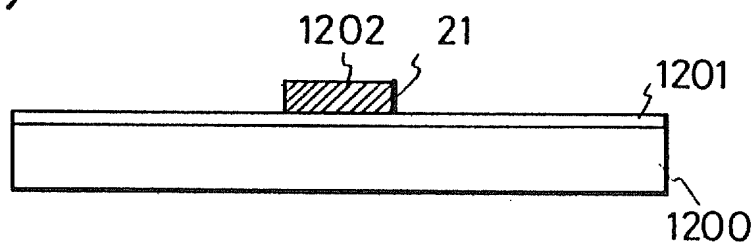


FIG. 26(B)

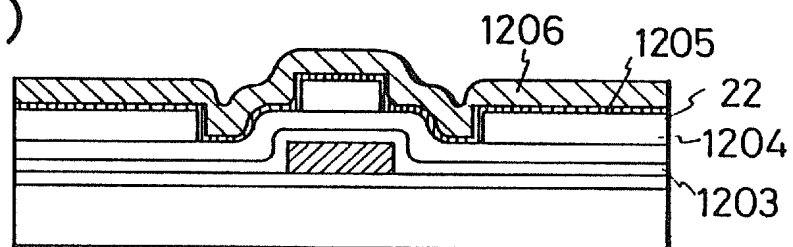


FIG. 26(C)

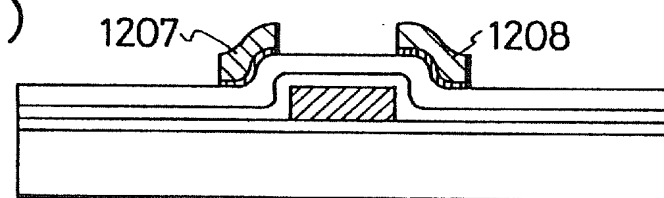


FIG. 26(D)

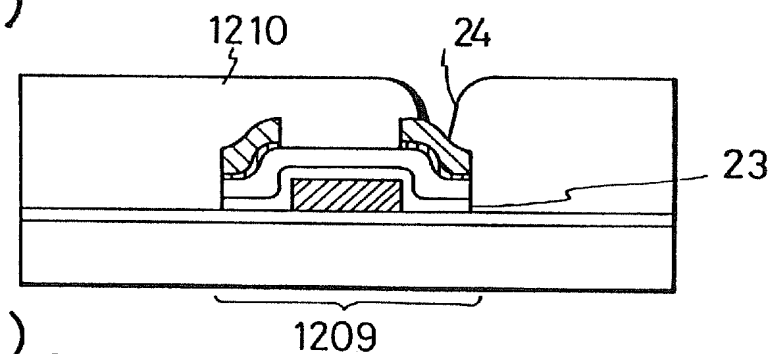


FIG. 26(E)

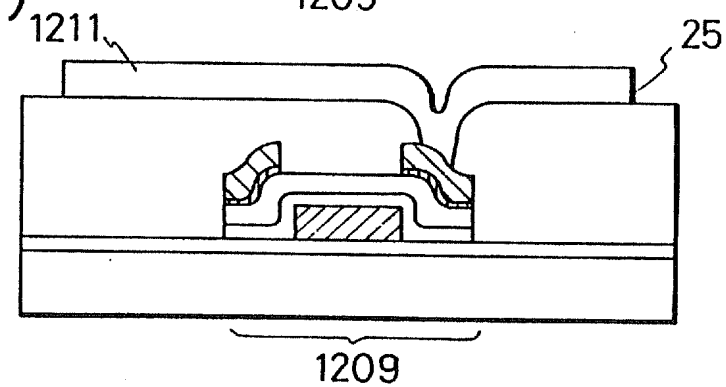


FIG. 27(A)

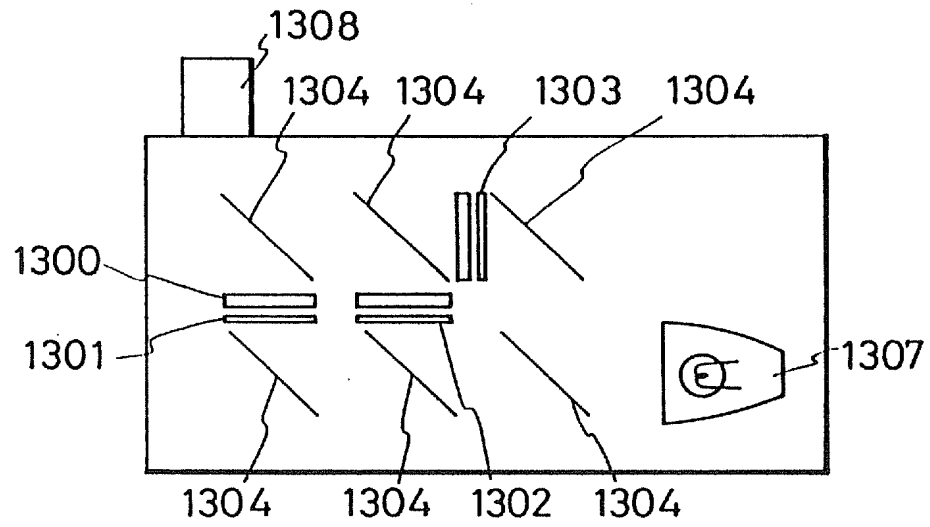


FIG. 27(B)

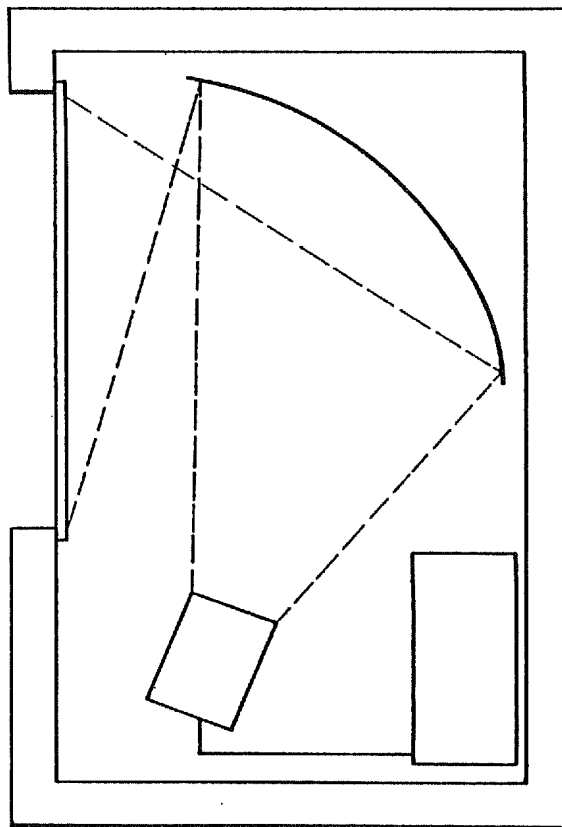


FIG. 28(A)

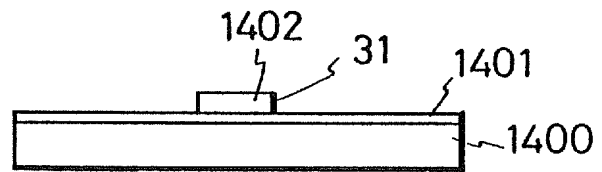


FIG. 28(B)

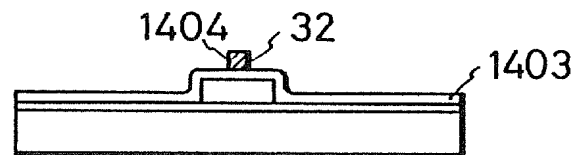


FIG. 28(C)

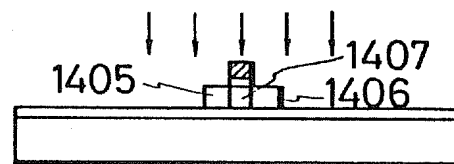


FIG. 28(D)

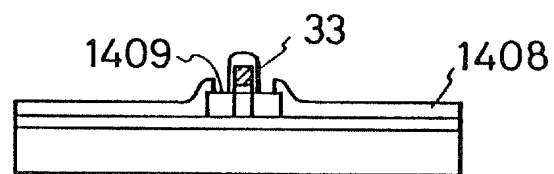


FIG. 28(E)

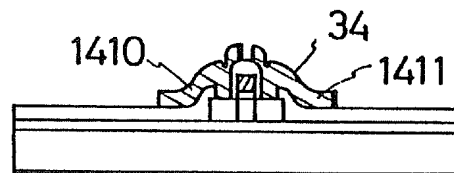


FIG. 28(F)

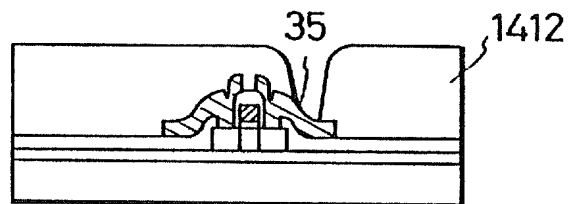


FIG. 28(G)

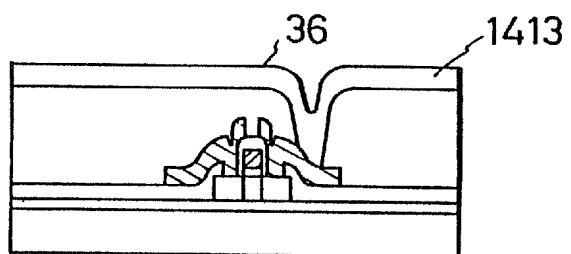


FIG. 29

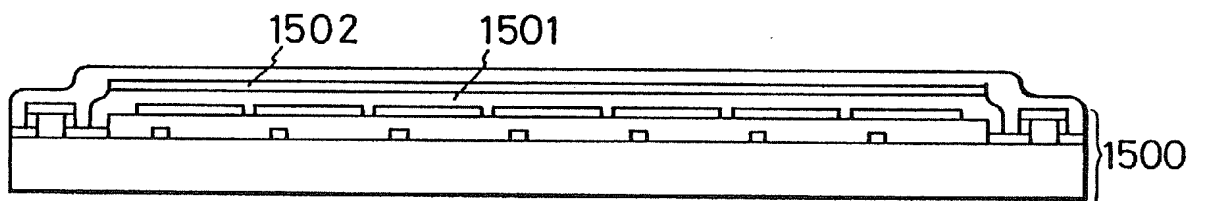


FIG. 30(A)

FIG. 30(B)

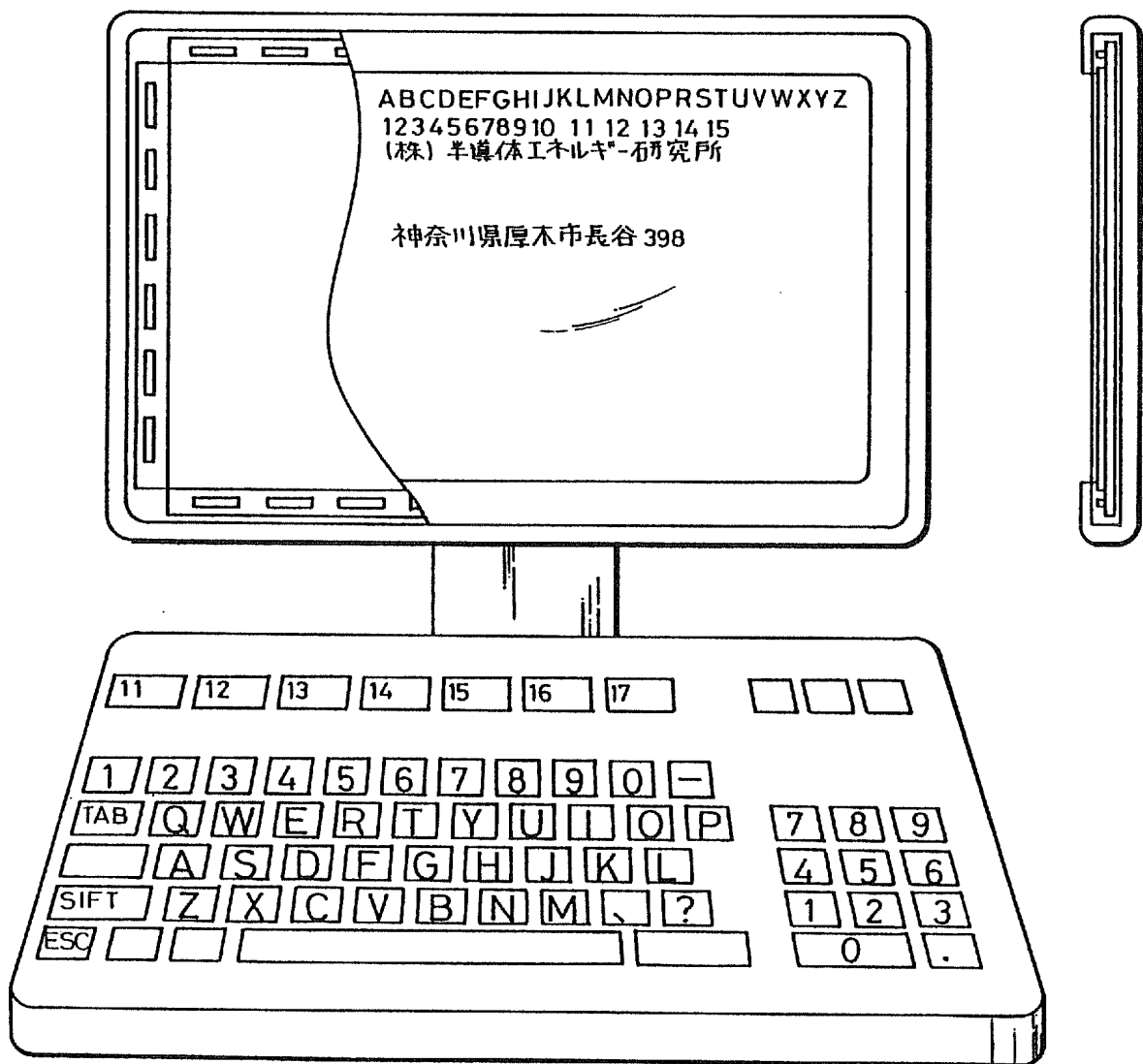


FIG. 31

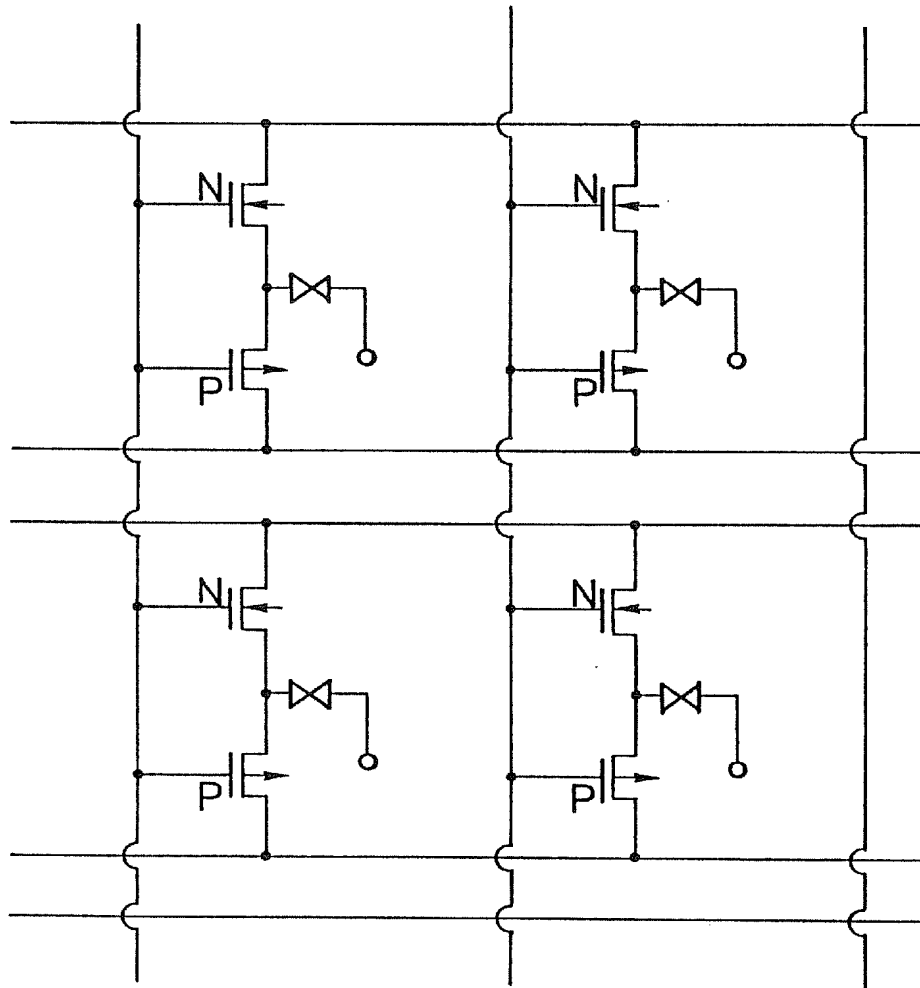


FIG. 32A

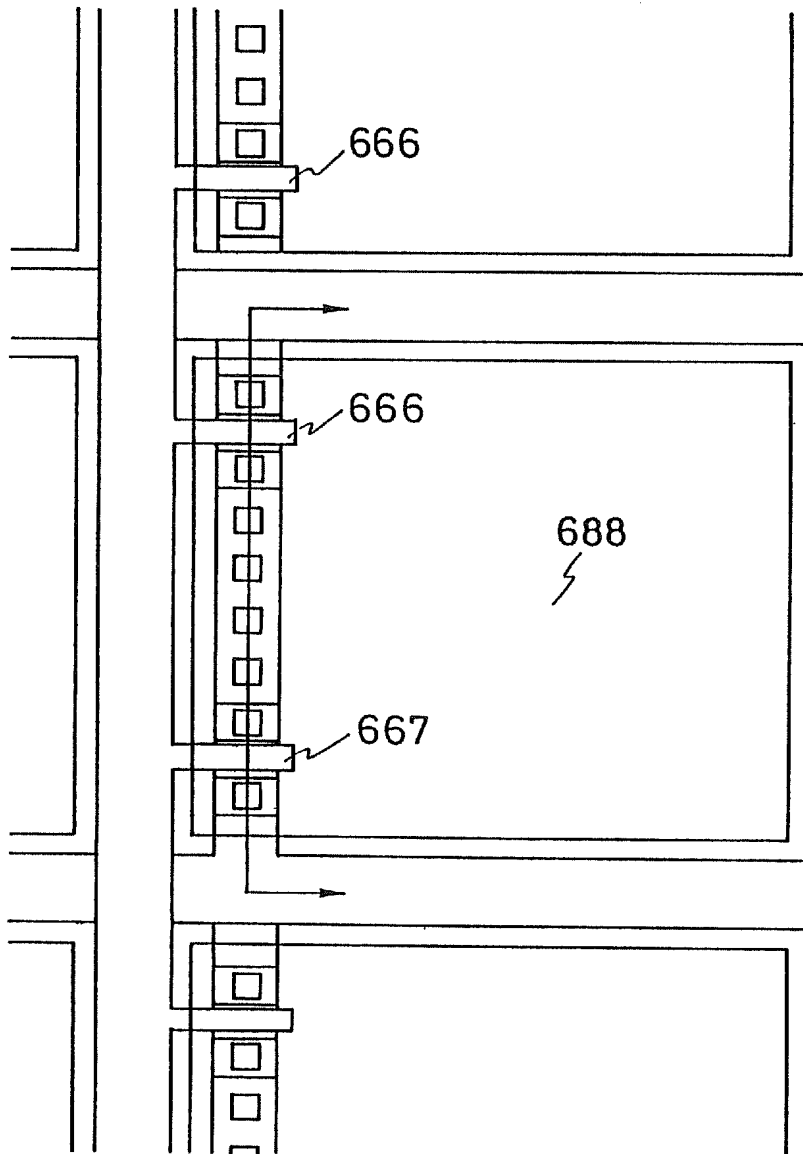


FIG. 32B

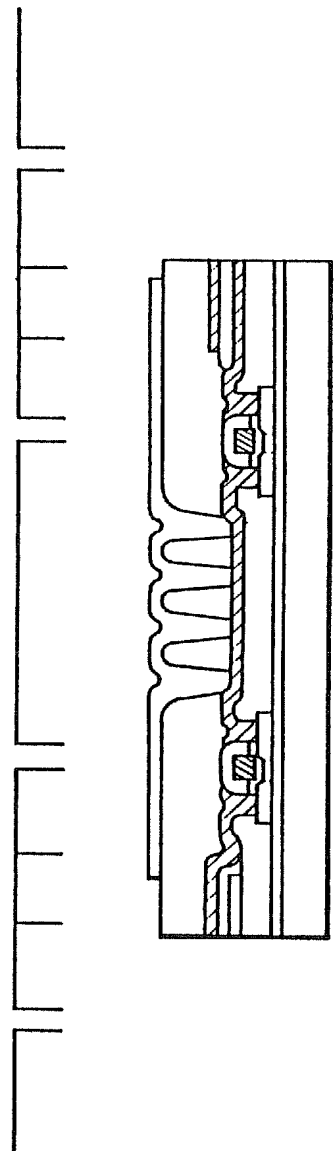


FIG. 33(A)

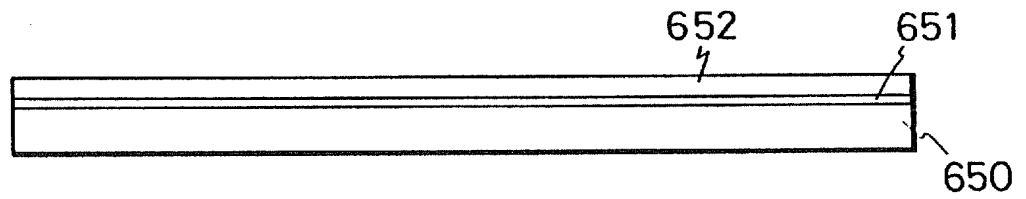


FIG. 33(B)

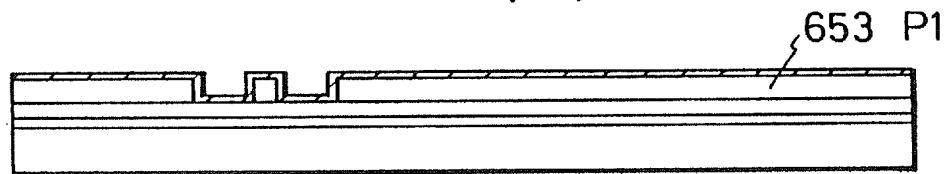


FIG. 33(C)

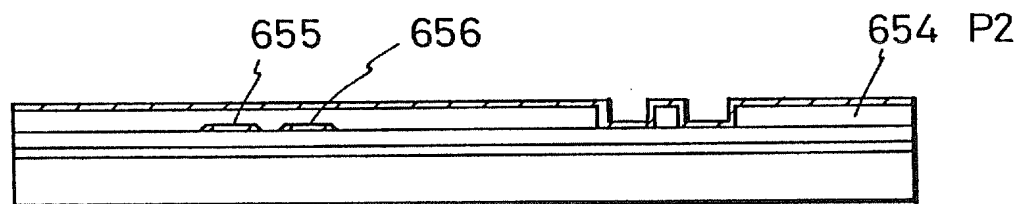


FIG. 33(D)

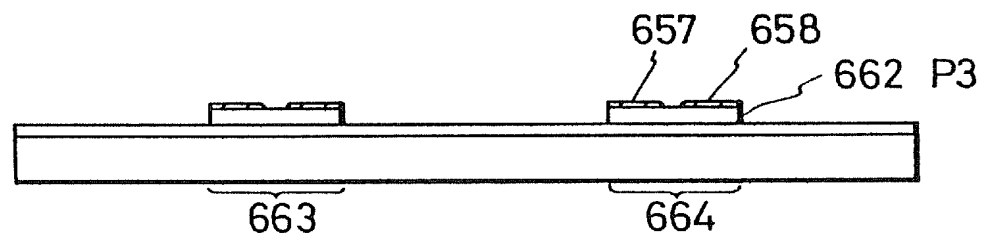


FIG. 33(E)

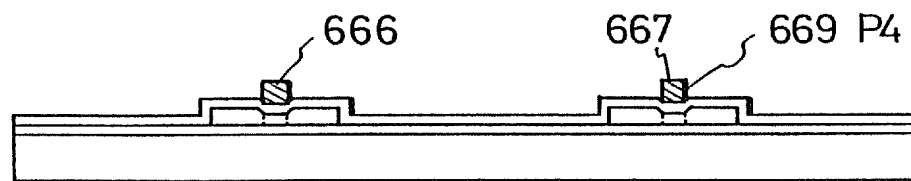


FIG. 33(F)

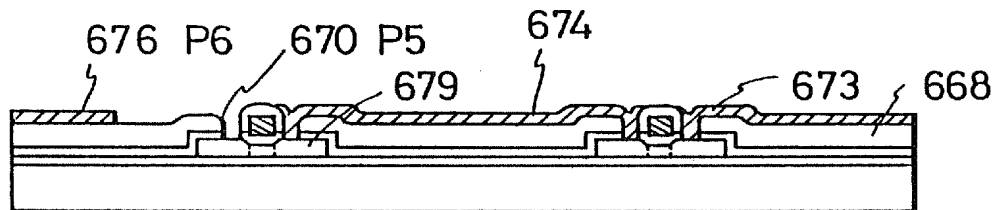


FIG. 33(G)

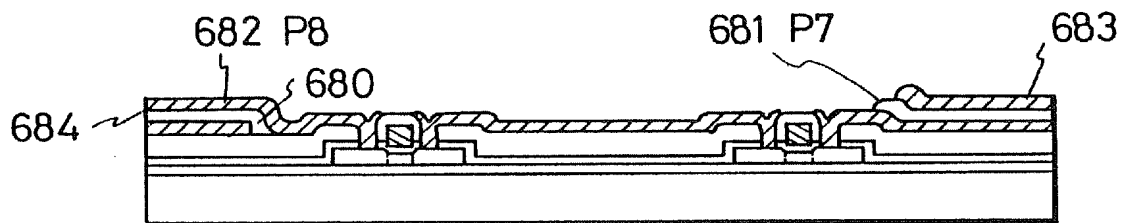


FIG. 33(H)

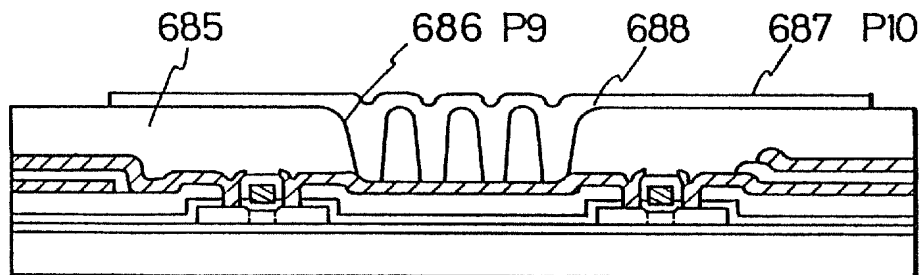


FIG. 34

COMPOSITE VIDEO INPUT (BLACK-AND-WHITE)

SYNCHRONIZATION SEPARATION

SYNCHRONIZING SIGNAL

PLL SYNCHRONIZATION TIMING GENERATION

COUNTER

CLK

VD ϕ V

COMPENSATION

A/D (6BIT)

356

352

SHIFT RESISTOR (H)

LATCH

6BIT DATA LATCH

358

6BIT MAGNITUDE COMPARATOR

MC

MC

MC

MC

350

351

353

360

SHIFT RESISTOR PROVIDED WITH BUFFER(V)

355

HD ϕ H

354

357

359

361

362

363

364

365

366

367

368

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371

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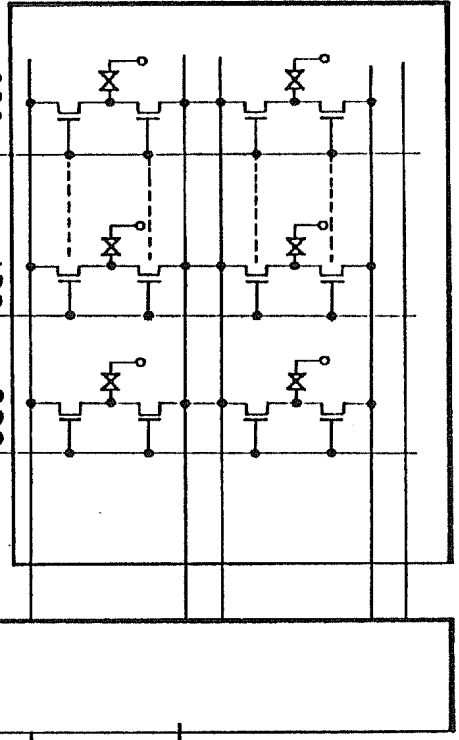


FIG. 35(A)

$f = 5\text{KHz}$

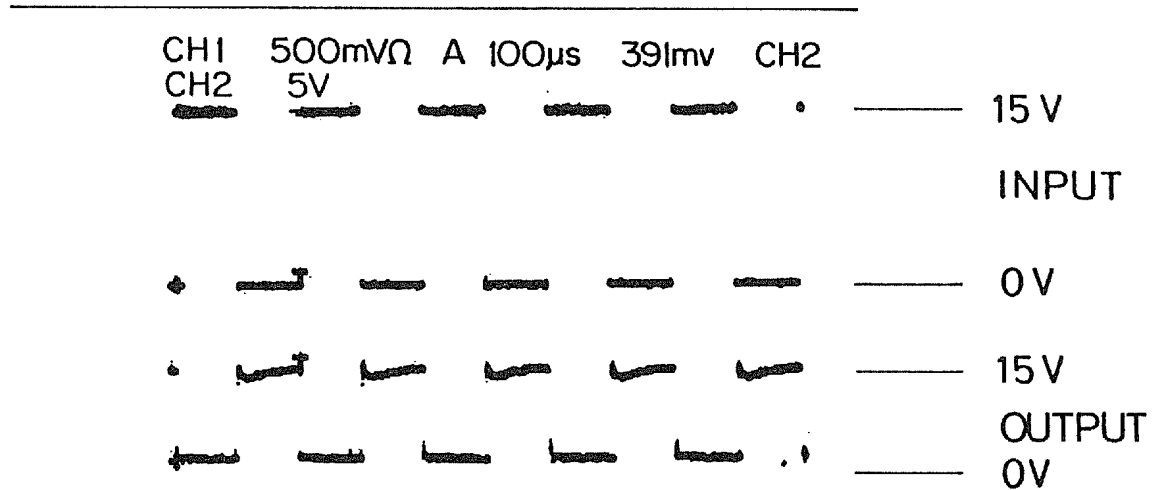


FIG. 35(B)

$f = 50\text{KHz}$

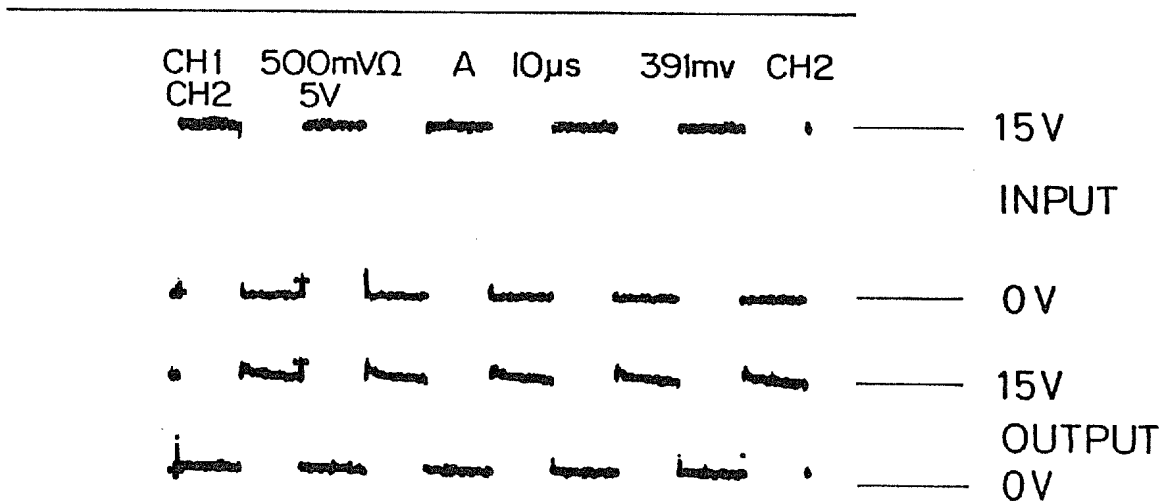


FIG. 35(C)

$f = 500 \text{ KHz}$

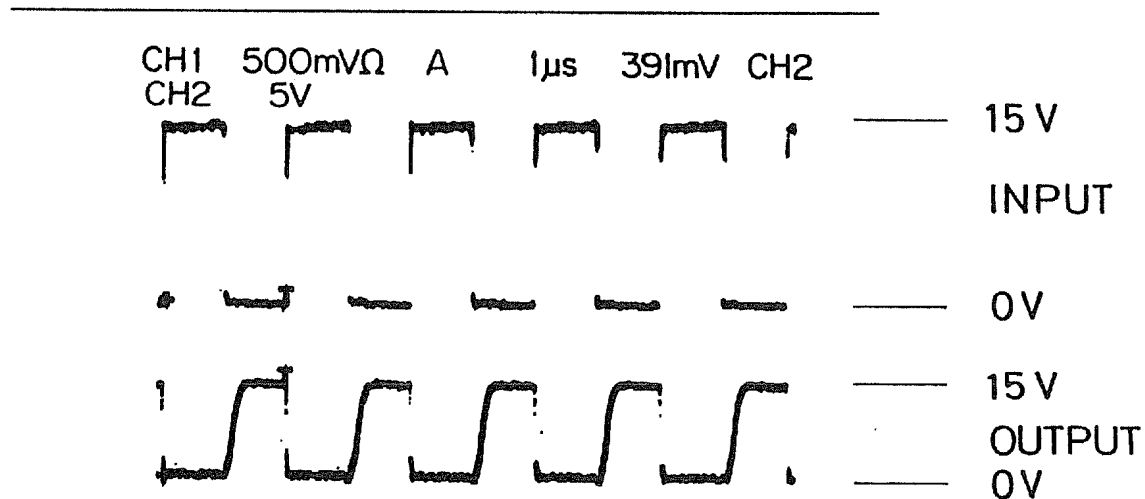


FIG. 35(D)

$f = 1 \text{ MHz}$

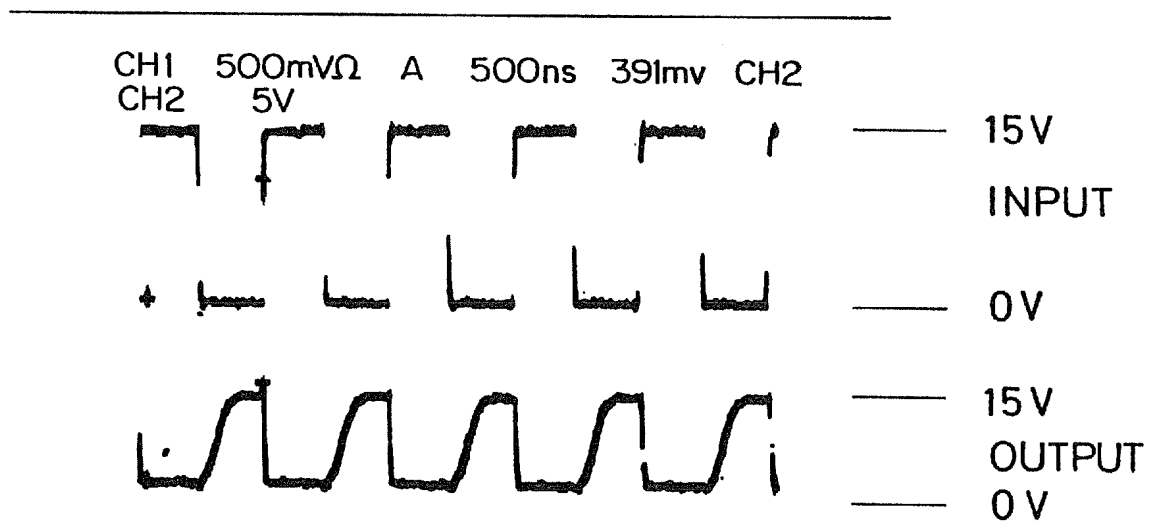


FIG. 36(A)

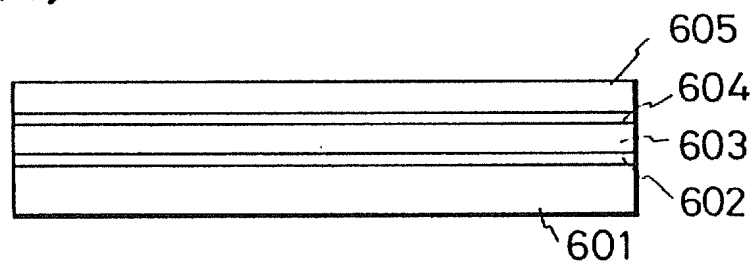


FIG. 36(B)

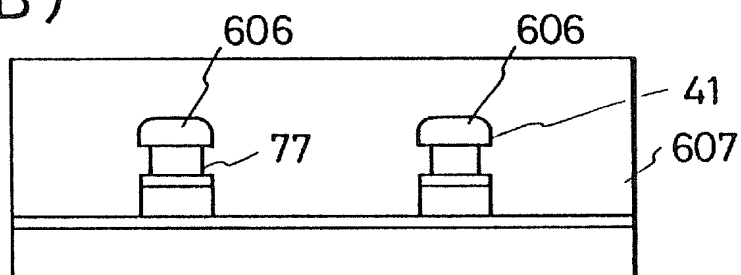


FIG. 36(C)

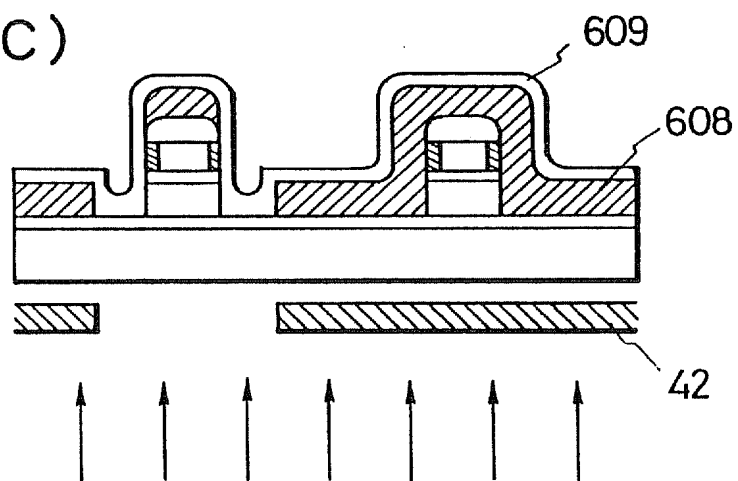


FIG. 36(D)

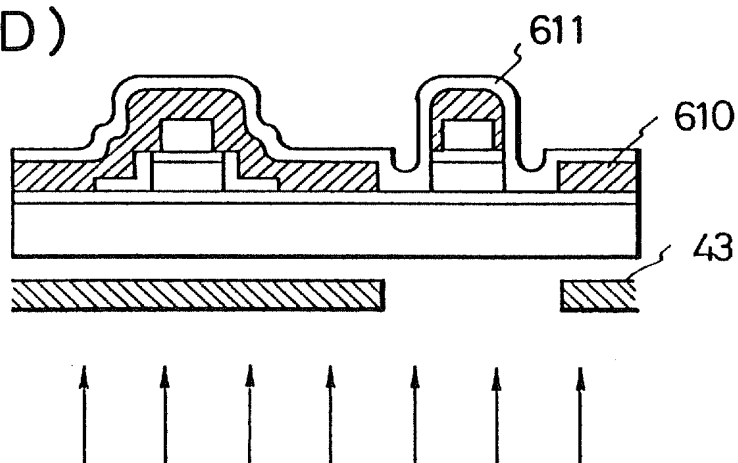


FIG. 36(E)

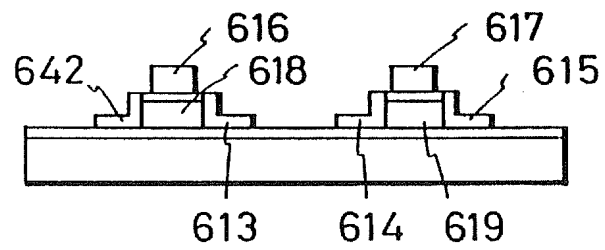


FIG. 36(F)

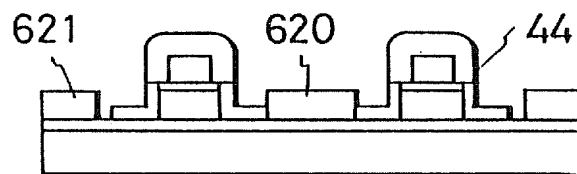


FIG. 36(G)

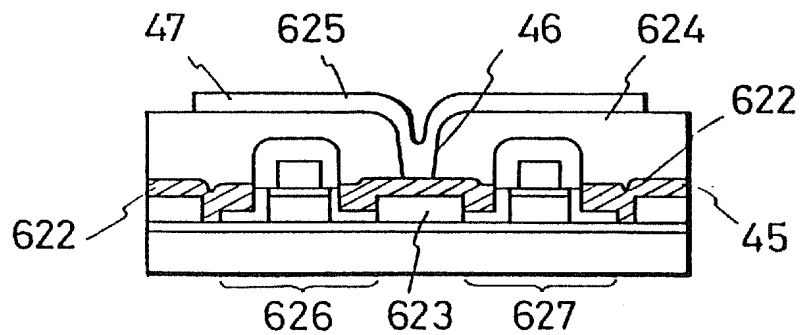


FIG. 37

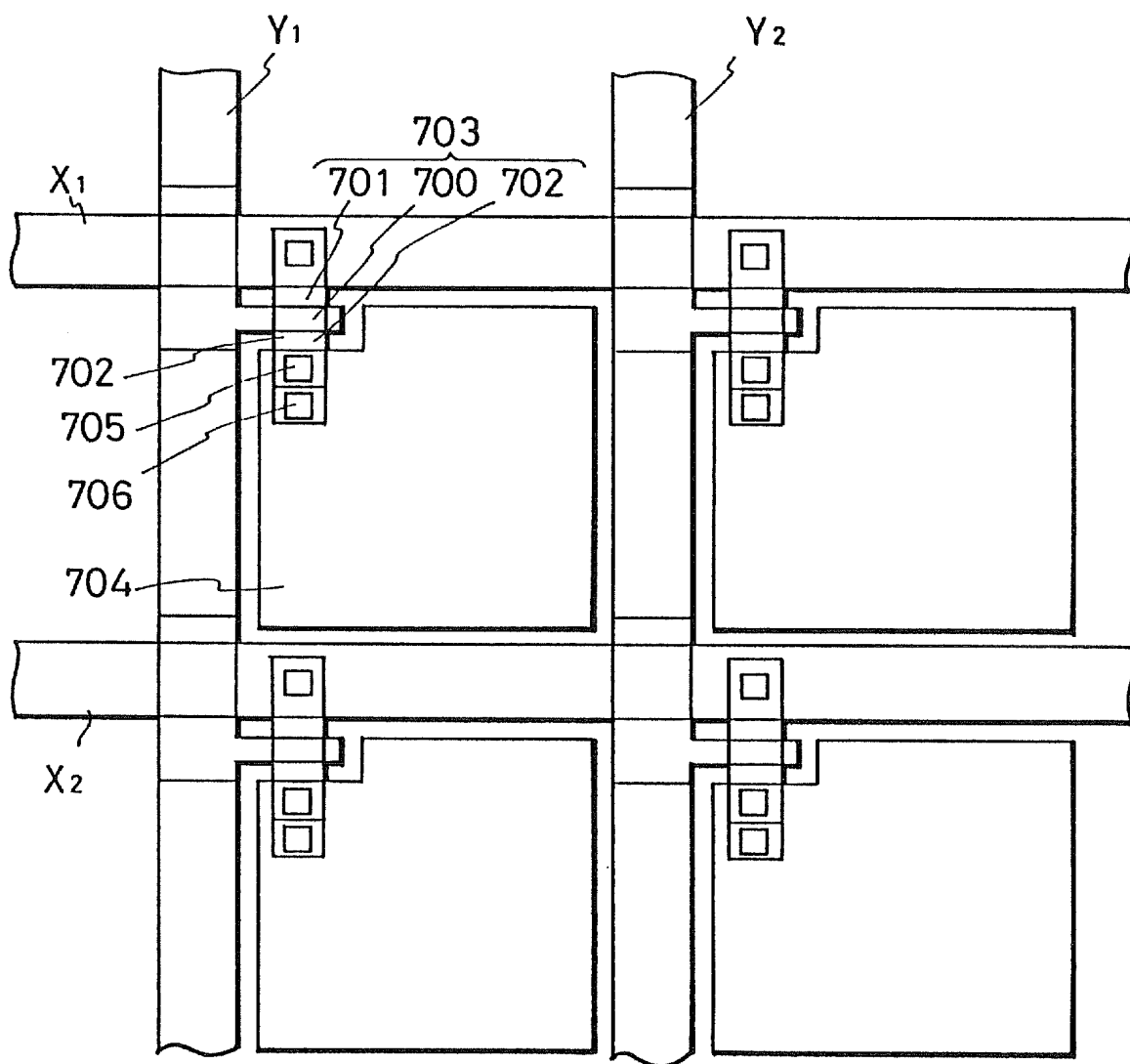


FIG. 38

